

Compal Confidential

PAGANI M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point

Date : 2011/11/22

Version 0.1

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address


Device	Address
PCH (Reserve)	1010 0110b


SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CLK EC_SMB_DATA	PCH_SMB_CLK PCH_SMB_DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMB_CLK PCH_SMB_DATA	PCH				V	V					V
PCH_SML_CLK PCH_SML_DATA	PCH										
PCH_SML1_CLK PCH_SML1_DATA	PCH						V				

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	CR+ Giga LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

SATA	DESTINATION
SATA0	HDD,JHDD1
SATA1	m-SATA,JMINI2
SATA2	ODD, JODD1
SATA3	None
SATA4	None
SATA5	None

Option	@	CONN@	PX@	
UMA	X	X	X	
DIS	X	X	V	

USB Port Table

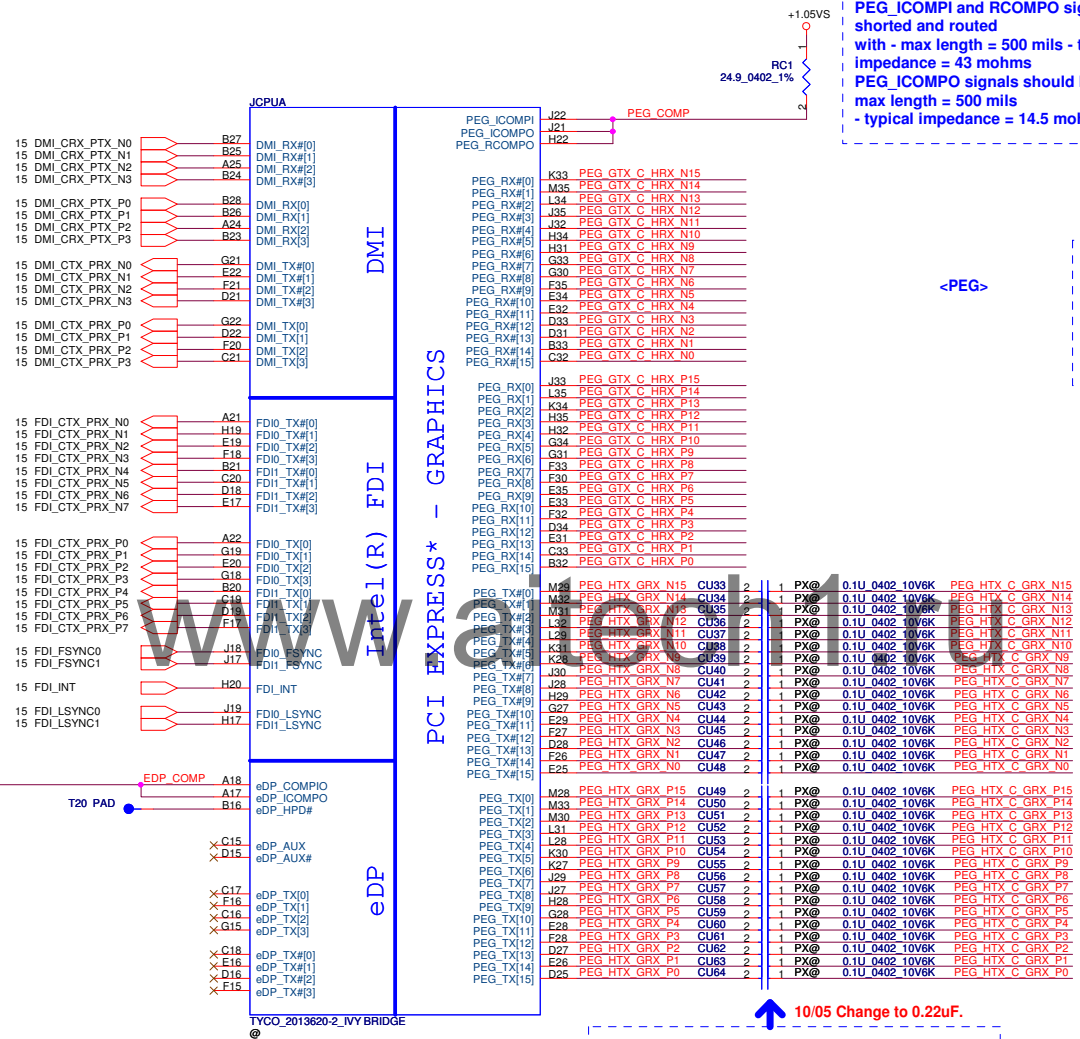
USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB3.0
		1	USB3.0
	UHCI1	2	USB3.0
		3	USB2.0 FRP
	UHCI2	4	X
		5	m-SATA
EHCI2	UHCI3	6	X
		7	X
	UHCI4	8	Camera
		9	USB2.0 and sleep charger
	UHCI5	10	minPCIE-WLAN/BT
		11	X
	UHCI6	12	X
		13	X

USB 3.0	Port	3 External USB Port
	0	USB3.0
	1	USB3.0
	2	USB3.0(SB)

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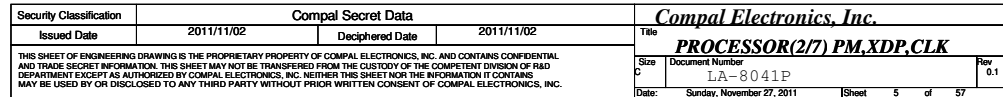
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

NOTE:eDP_COMPIO and eDP_ICOMPO should not be left floating even if Internal Graphic is disabled since they are shared with other interfaces



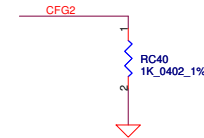
Typ- suggest 220nF. The change in AC capacitor value from 180nF to 265nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)
11/23 AC-coupling capacitor is 0.1u.Chelsea only support GEN2.

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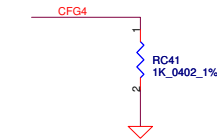
CFG Straps for Processor

change to install

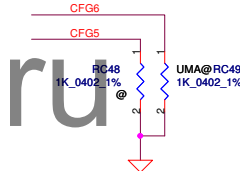


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>* 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>

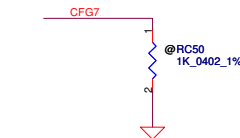
change to install



Display Port Presence Strap	
CFG4	<p>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIE Port Bifurcation Straps	
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>* 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>



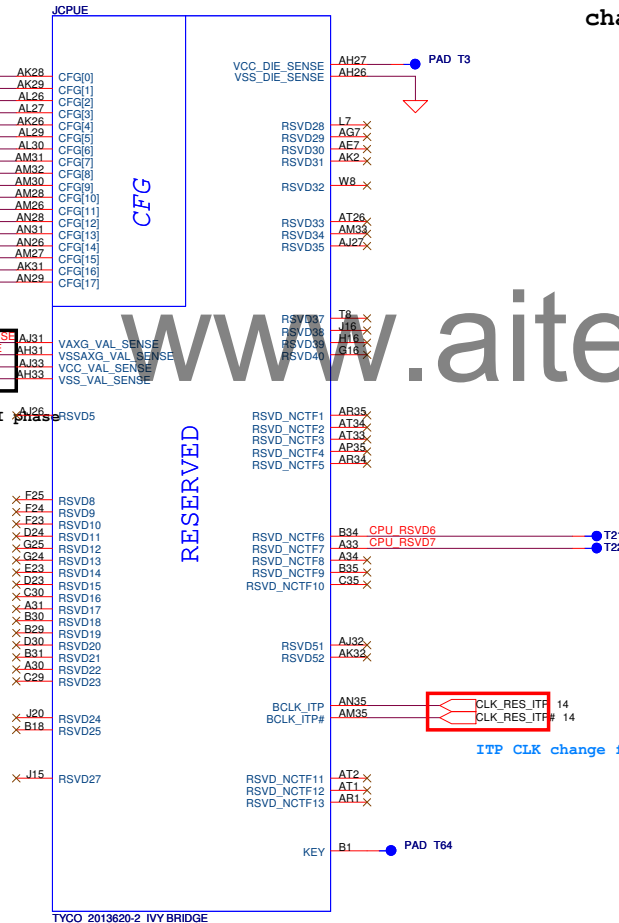
PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Train immediately following xRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

Change to part G.

2011.10.18 delete XDP resistor
just reserve test point for XDP.



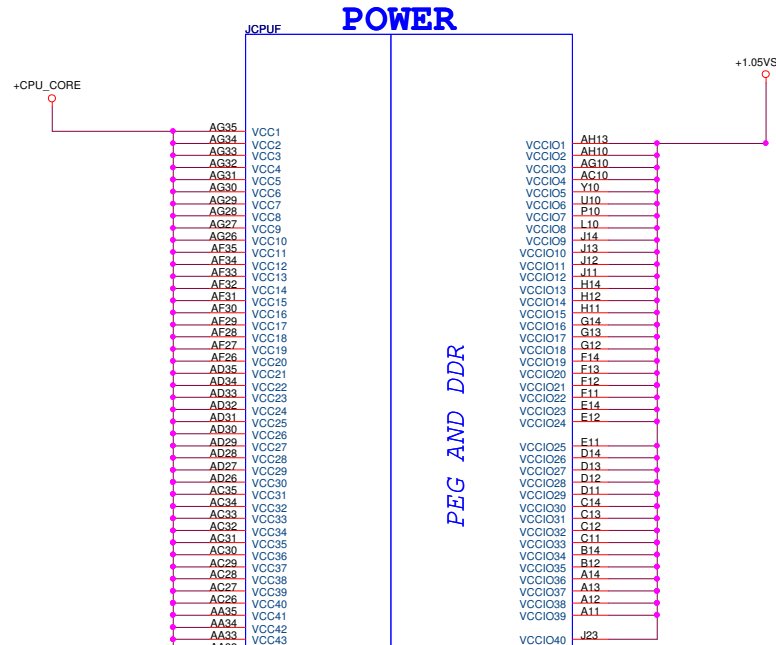
Just modify PWR to correct ,
didn't change net-name to save layout time; must modify on SI phase



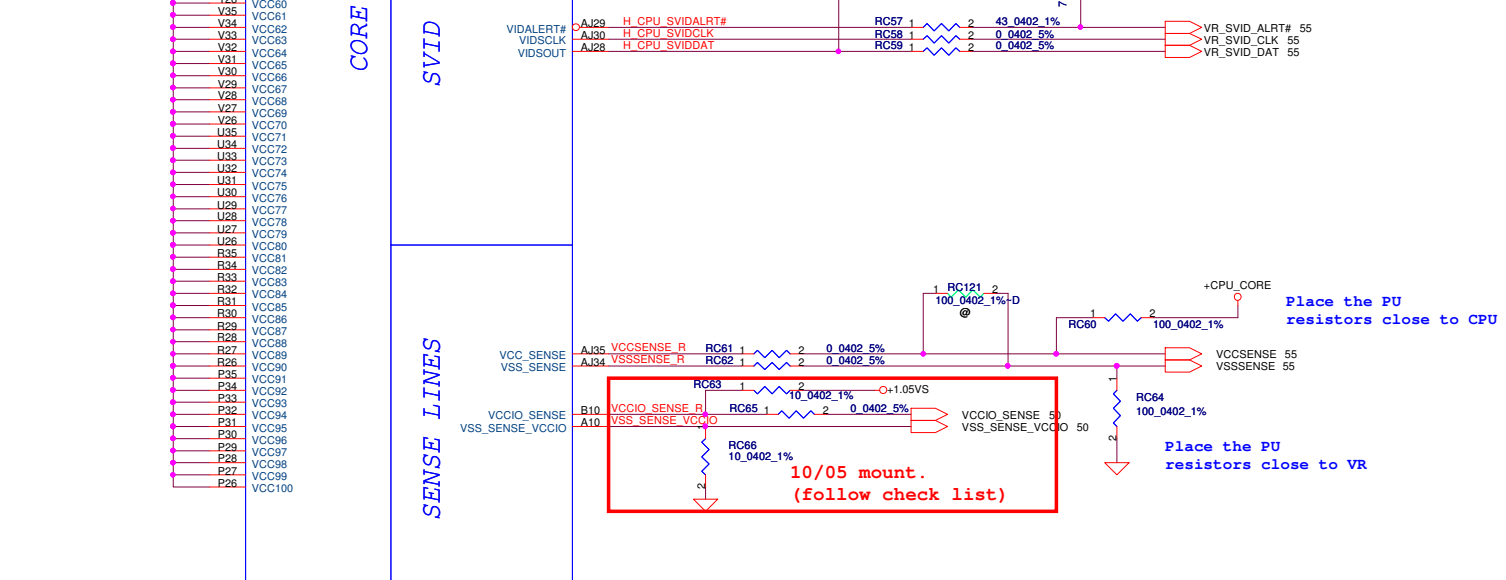
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				Size	Document Number		Rev 0.1
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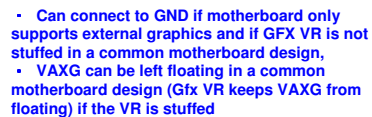
PROCESSOR(4/7) RSVD,CFG



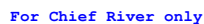
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TYCO_2013620-2_IVY BRIDGE				Compal Secret Data		Compal Electronics, Inc.	
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+VGFX_CORE



M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

10/03 add +V DDR REFB

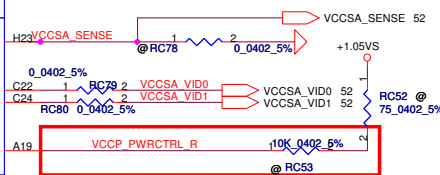


Follow DG 0.71 page 6



**Delete CC25 330U cap 10.19
(after check with power)**

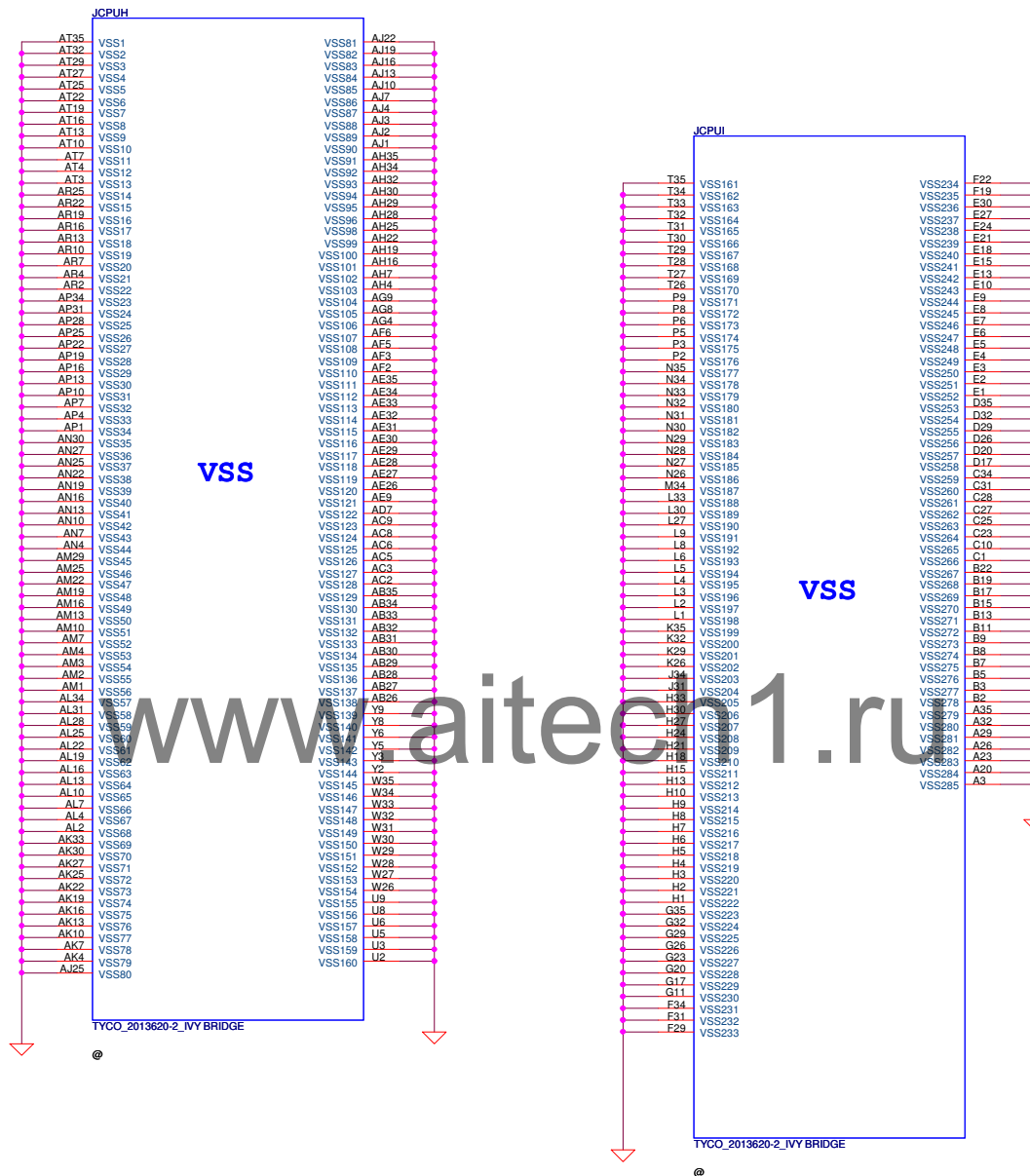
11/21 follow PBL22 design remove 10u*2, 1U*



CPU EDS descript as follow:
For Chief River platforms this pin
should not be used.

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

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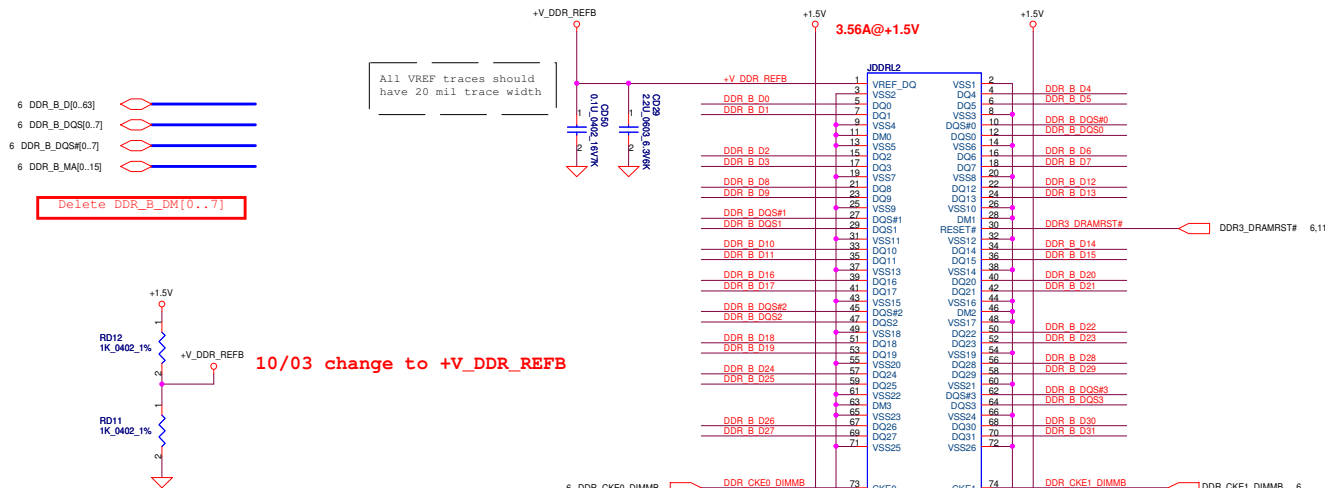
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DDR3 SO-DIMM A

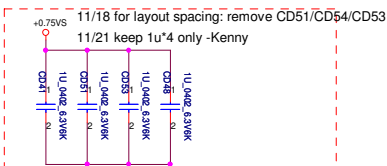


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				DDRIII DIMM	
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10/03 change to +V_DDR_REFB

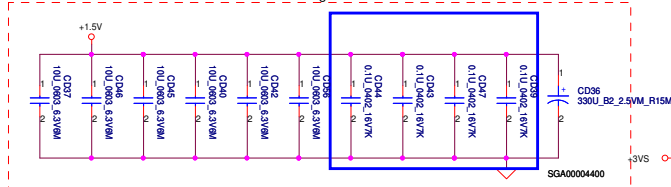


Layout Note:
Place near JDIMM1.203 & JDIMM1.204

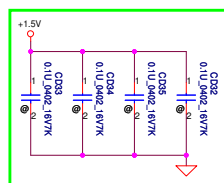


Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



DDR3 SO-DIMM B

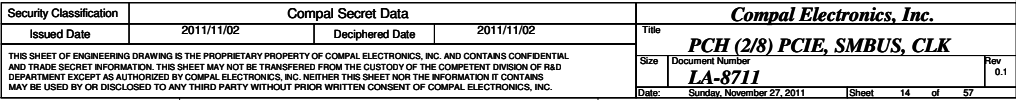


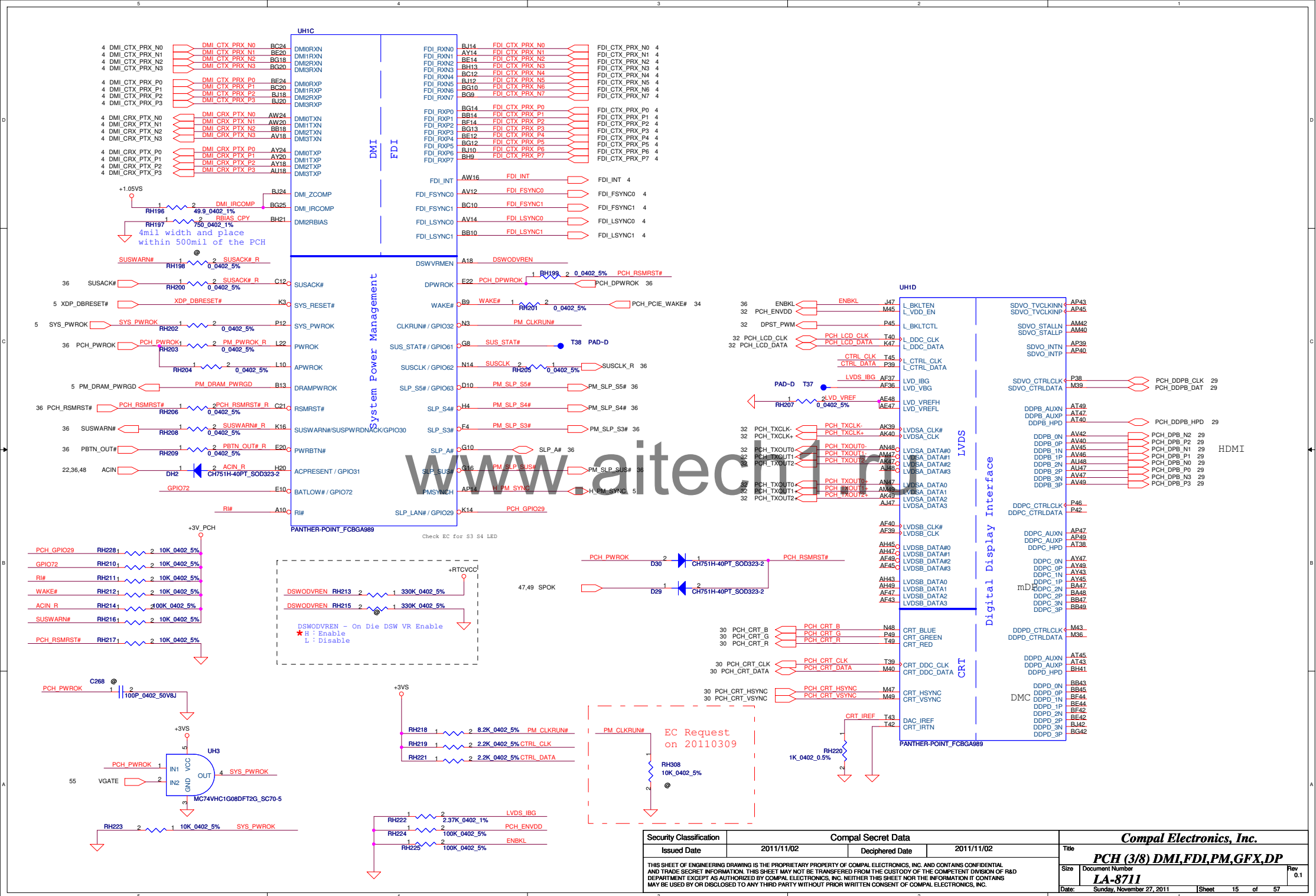
SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

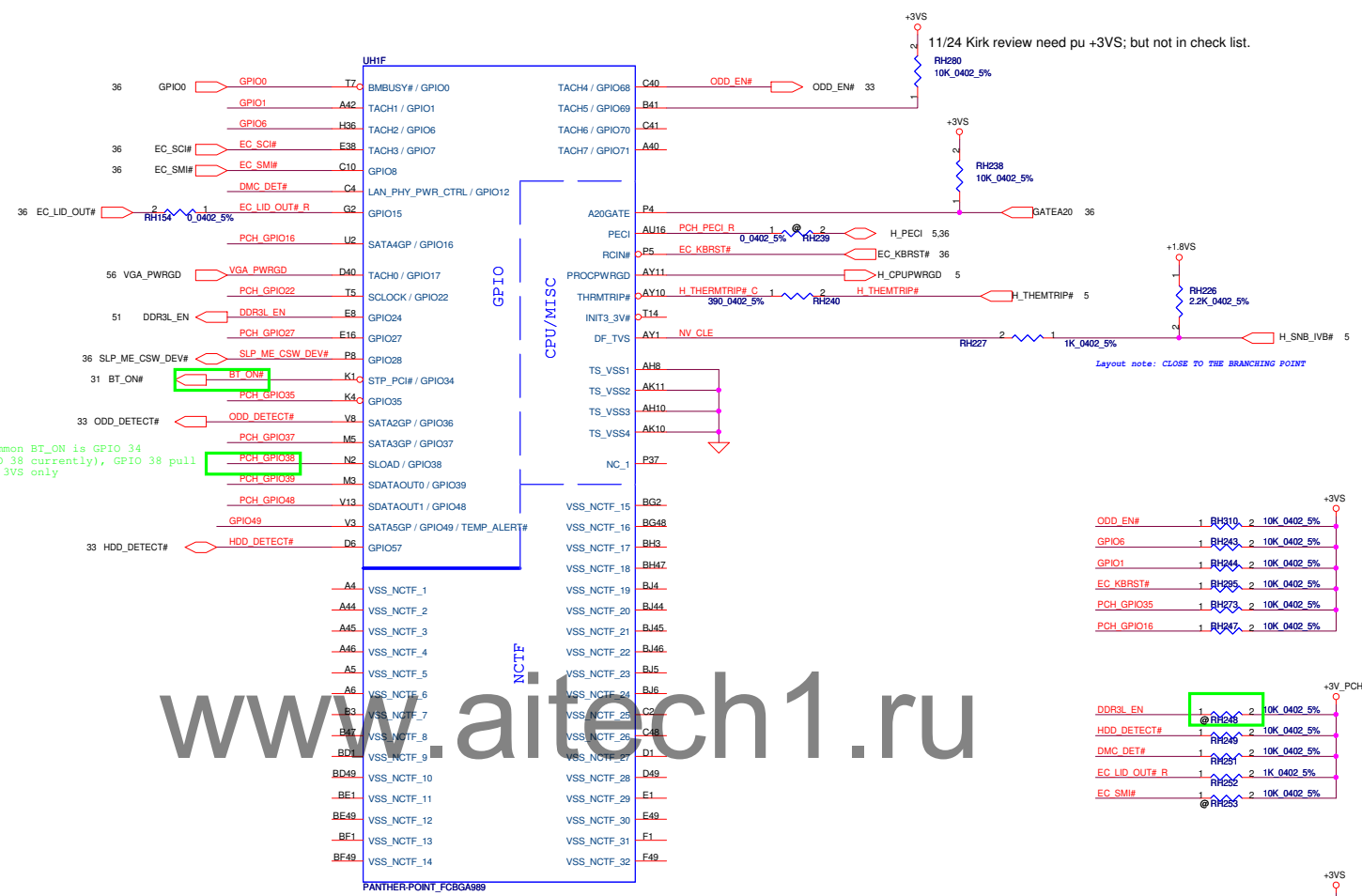
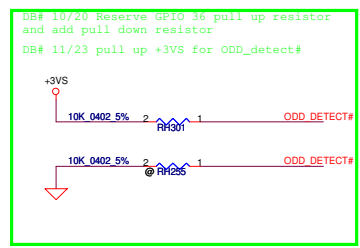
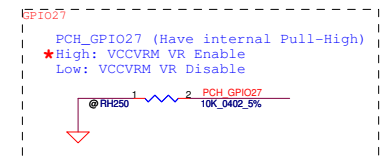
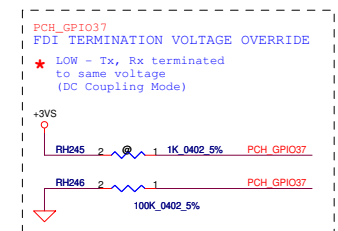
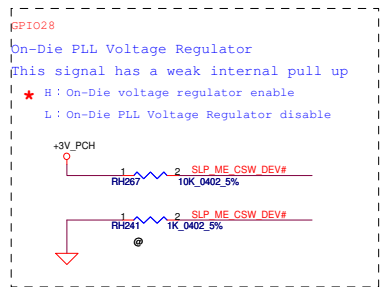
10/05 change to PH.

Standard
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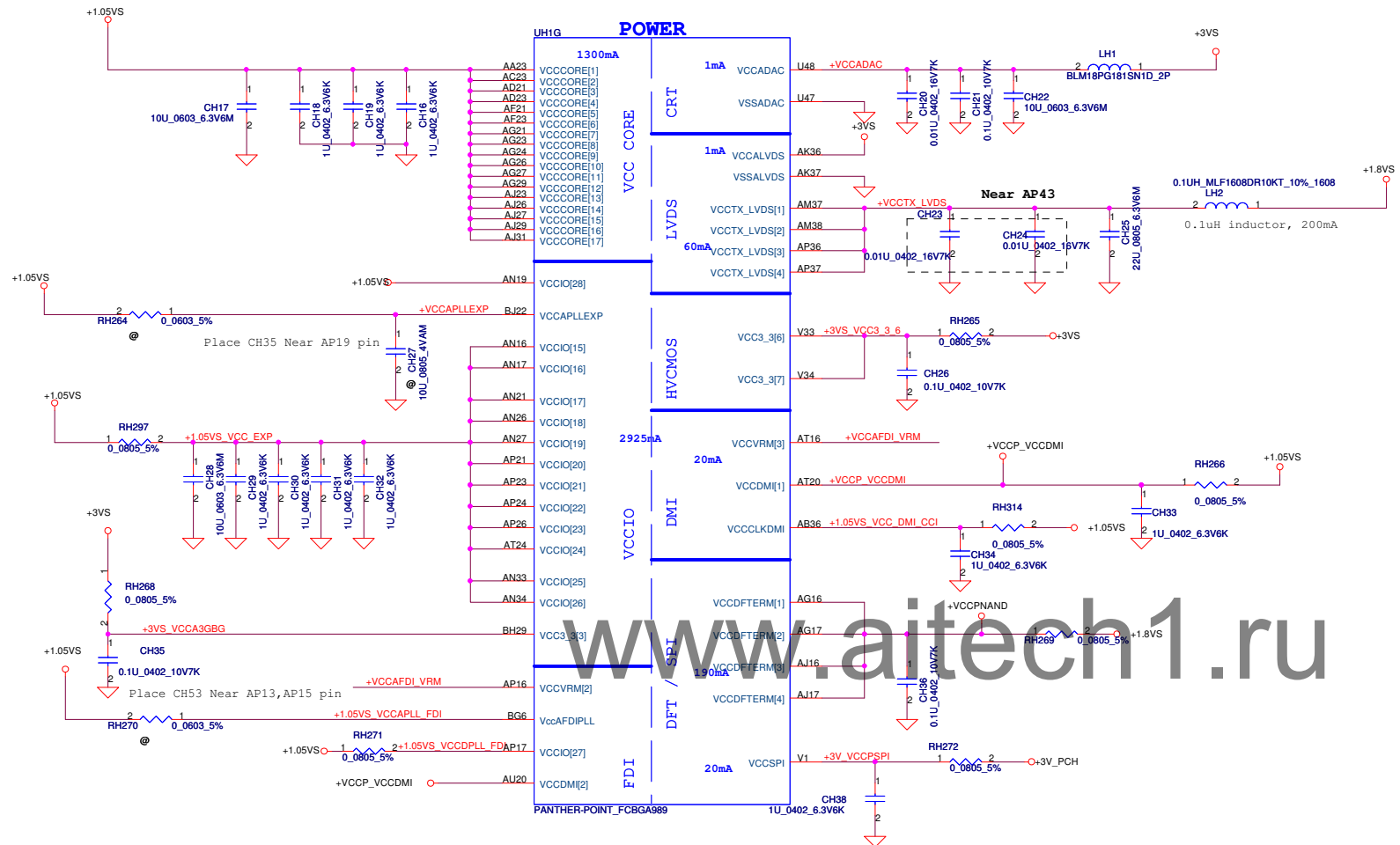






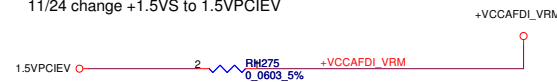
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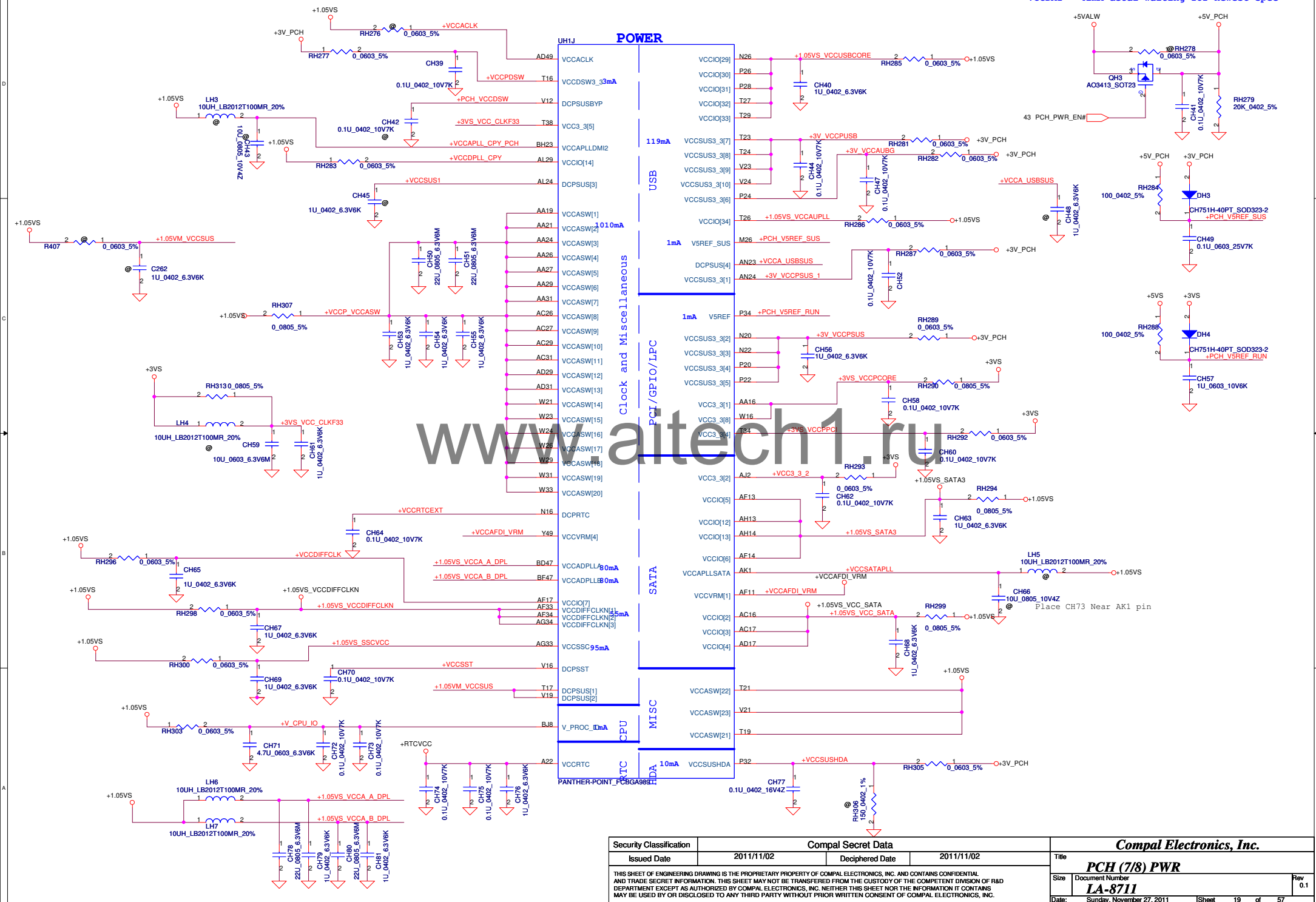
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

11/24 change +1.5VS to 1.5VPCIEV

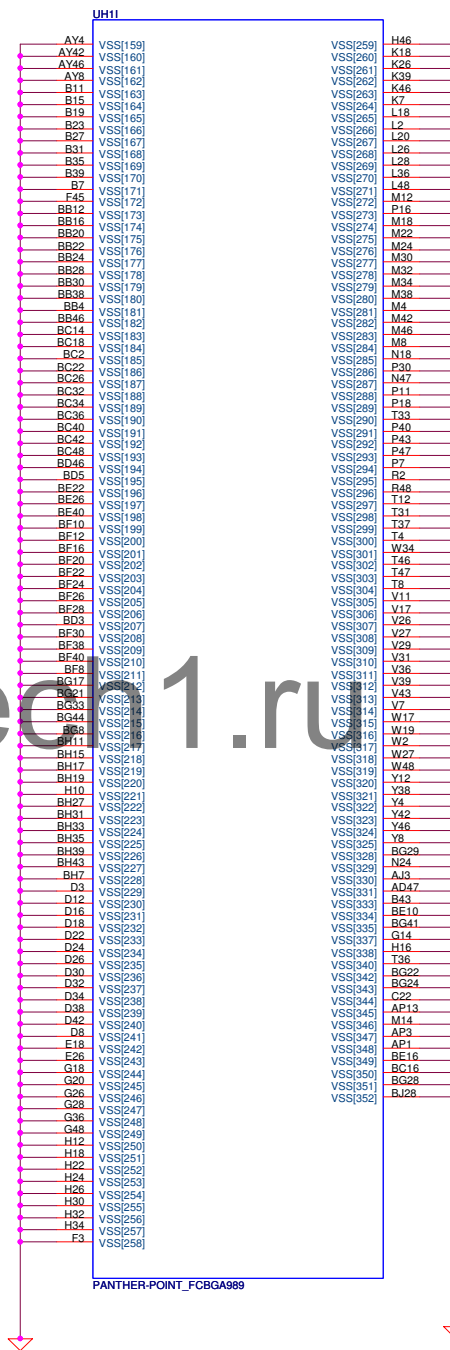
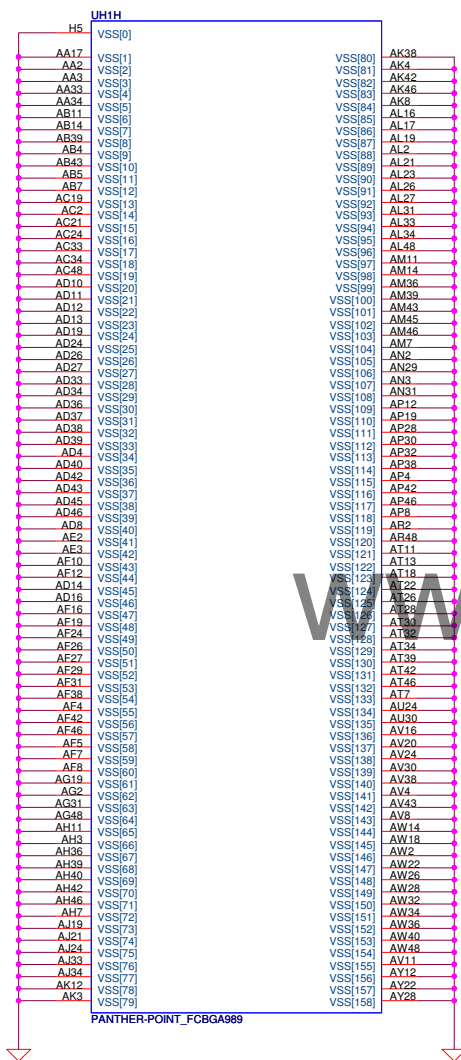


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VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

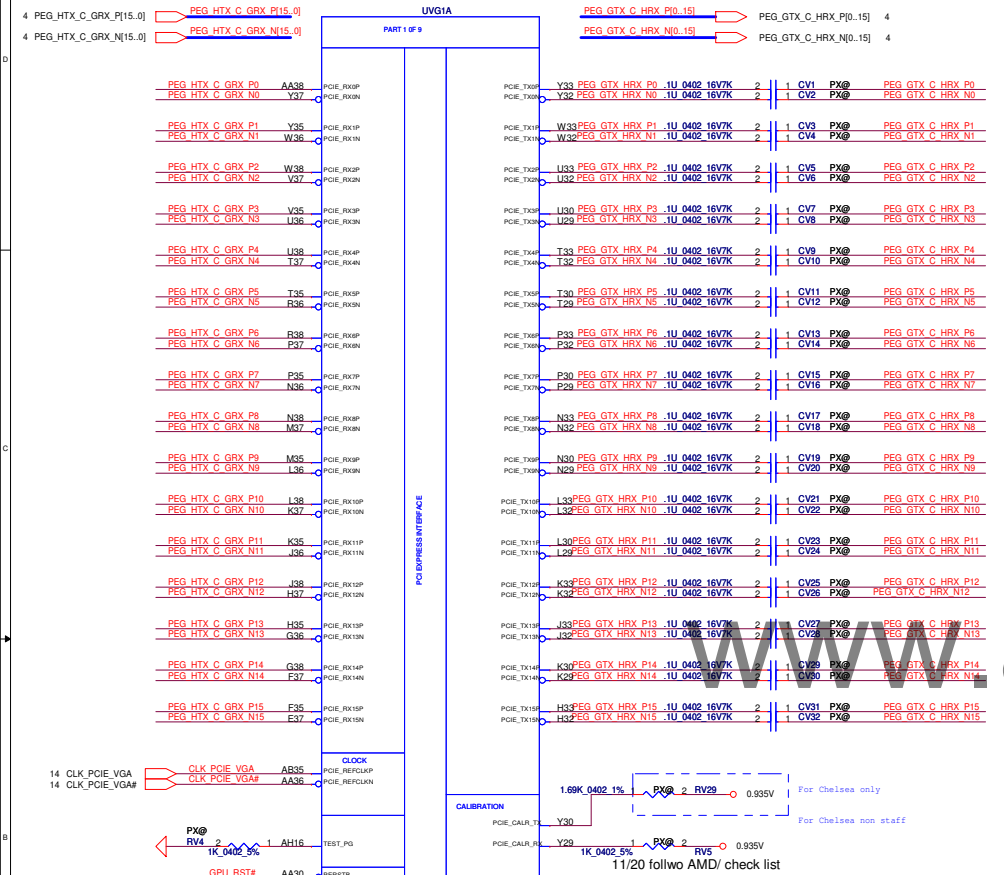


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					LA-8711	
Date:					Sunday, November 27, 2011	
					Sheet 19 of 57	

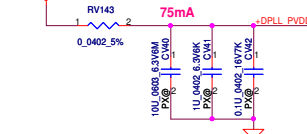


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Issued Date	2011/11/02	Deciphered Date	2011/11/02	Title	PCH (8/8) VSS
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					LA-8711
				Rev	0.1
				Date:	Sunday, November 27, 2011
				Sheet	20 of 57

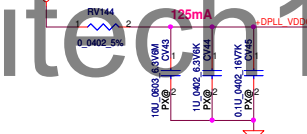
LVDS Interface



(1.8V@237mA for display use DP_VDDR)



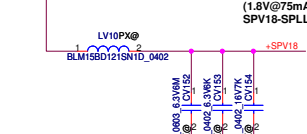
(0.935V@222mA DP_VDDC)



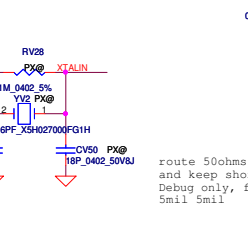
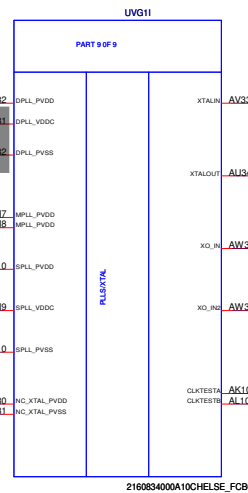
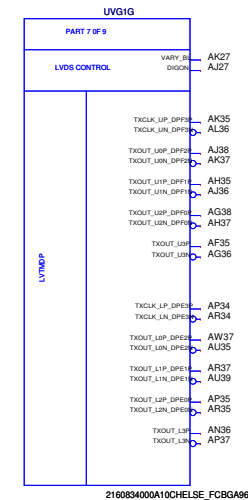
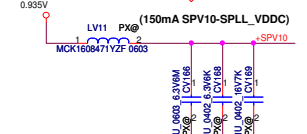
(M97, Broadway and Madison: 1.8V@150mA MPV18-MPLL_PVDD)



(1.8V@75mA SPV18-SPLL_PVDD)



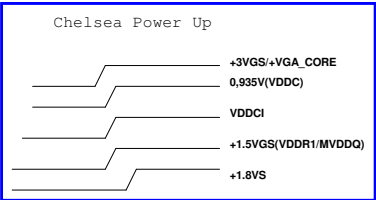
(150mA SPV10-SPLL_VDDC)



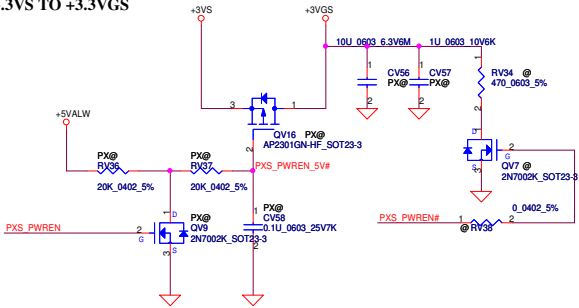
route 50ohms single-ended/100ohms diff and keep short Debug only, for clock observation, if not needed, DNI 5mil 5mil

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Size	C	Document Number	LA-8711	Rev 0.1
Date	Sunday, November 27, 2011	Sheet	21	of 57

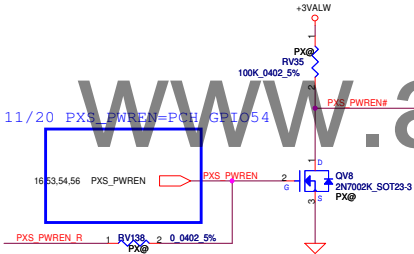
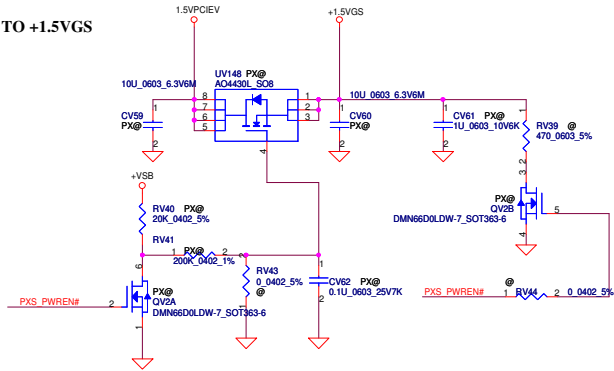
Name	FCH Pin Assignments
FE_GPIO0	GPIO191
FE_GPIO1	GPIO192
FE_PWRGD	GPIO28



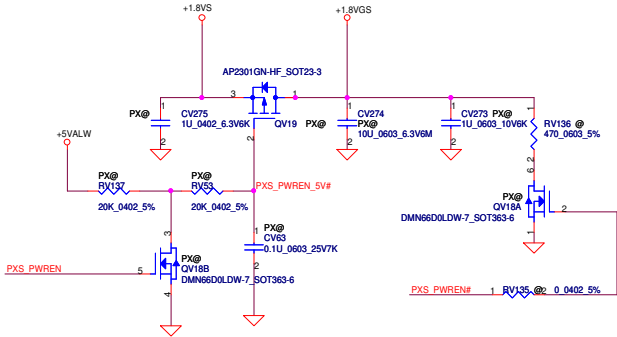
+3.3VS TO +3.3VGS



+1.5V TO +1.5VGS



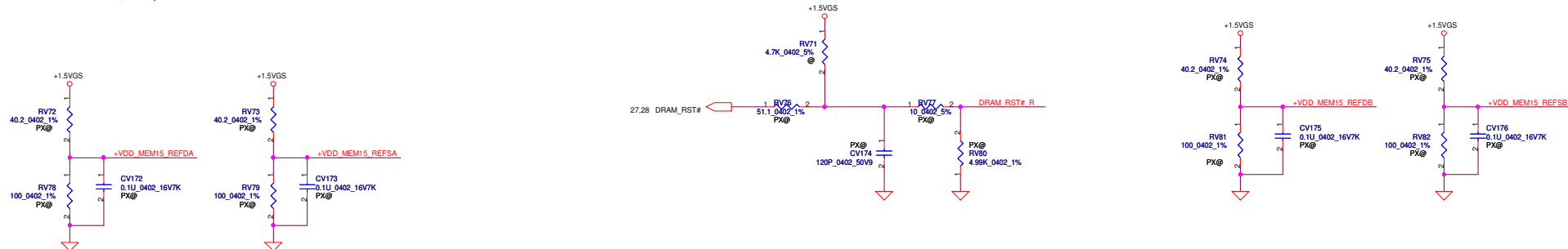
+1.8VS TO +1.8VGS





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This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

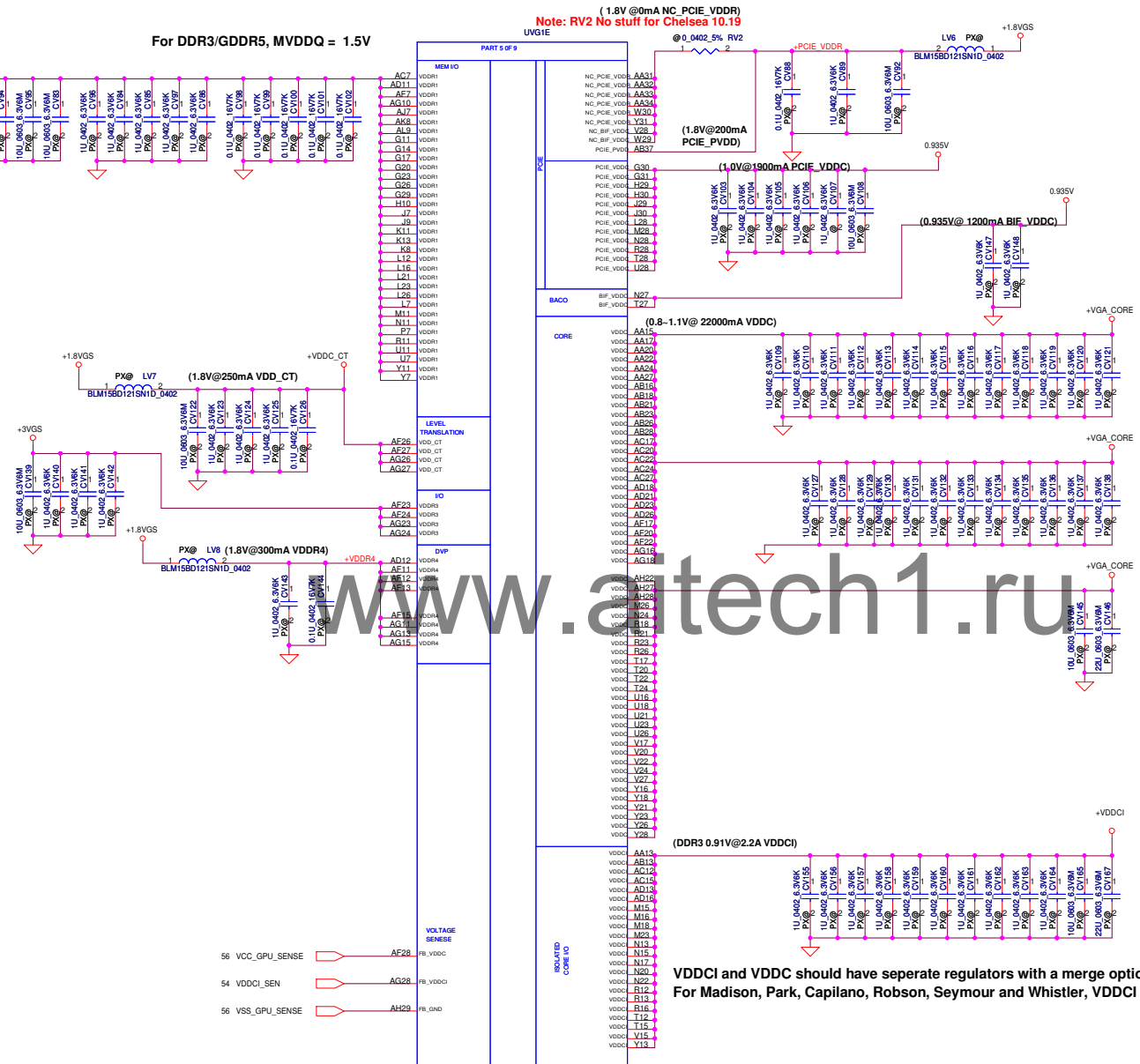
VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1



(1.8V @0mA NC_PCIE_VDDR)
Note: RV2 No stuff for Chelsea 10.13

For DDR3/GDDR5, MVDDQ = 1.5V

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

For Chelsea, Delete 2*10

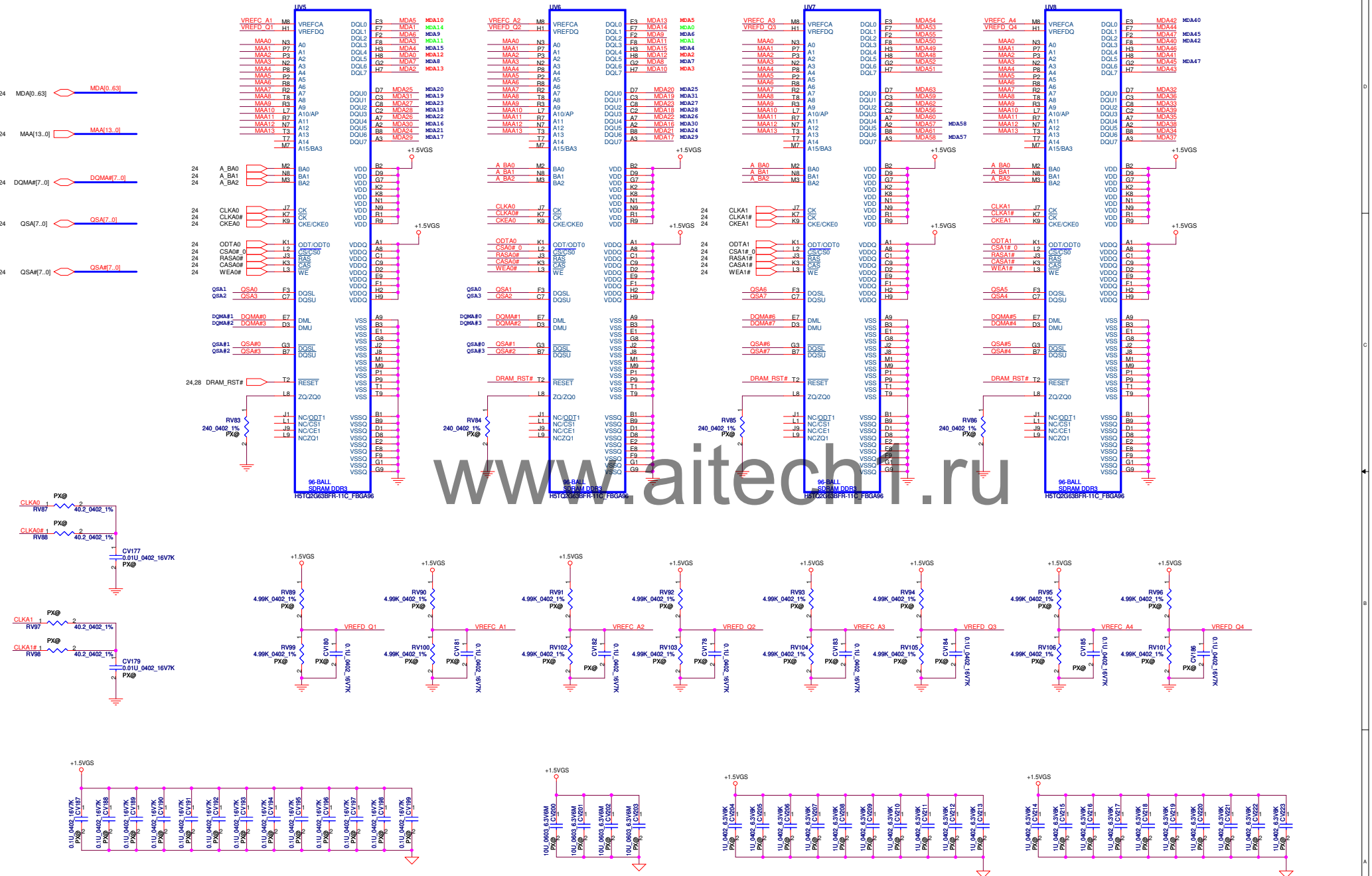
PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

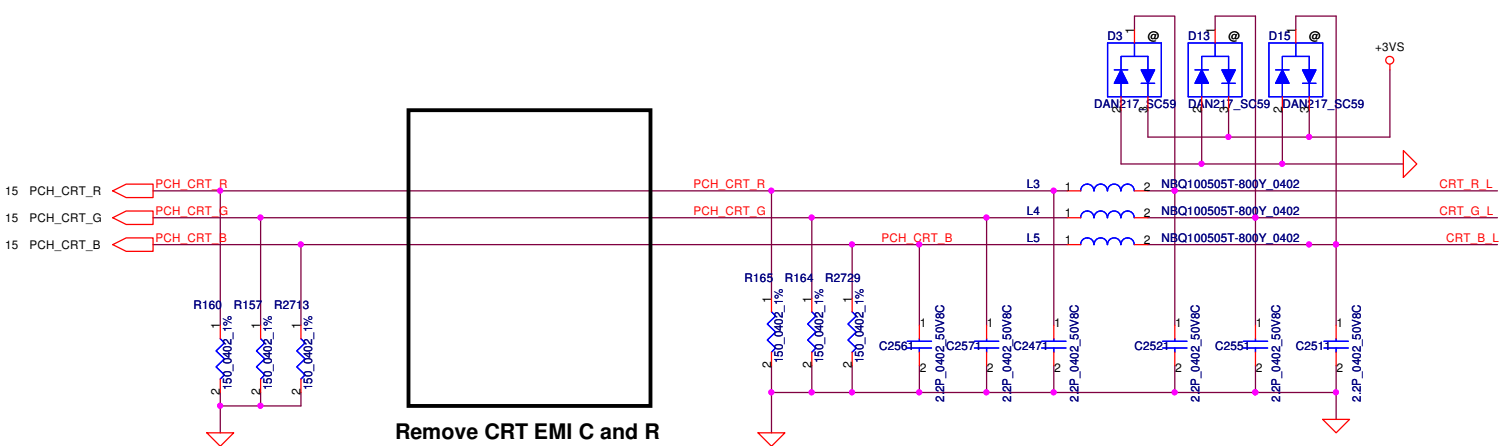
VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

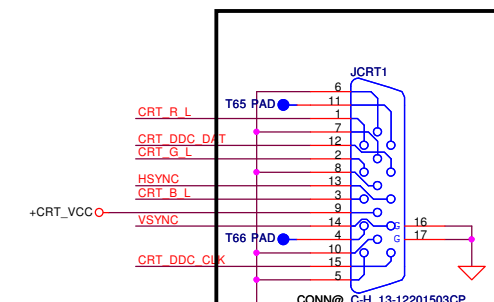
11/25 swap UV5.F8/ UV5.H8 =>MDA3/MDA0



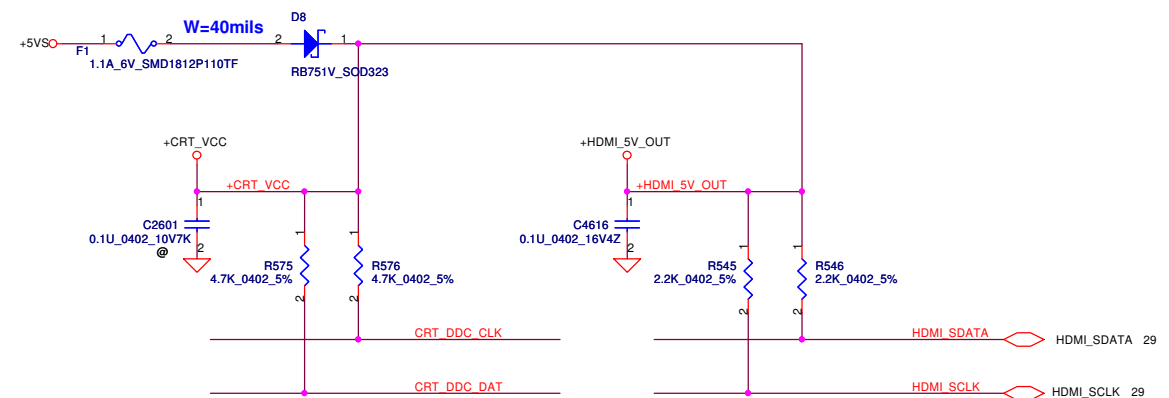
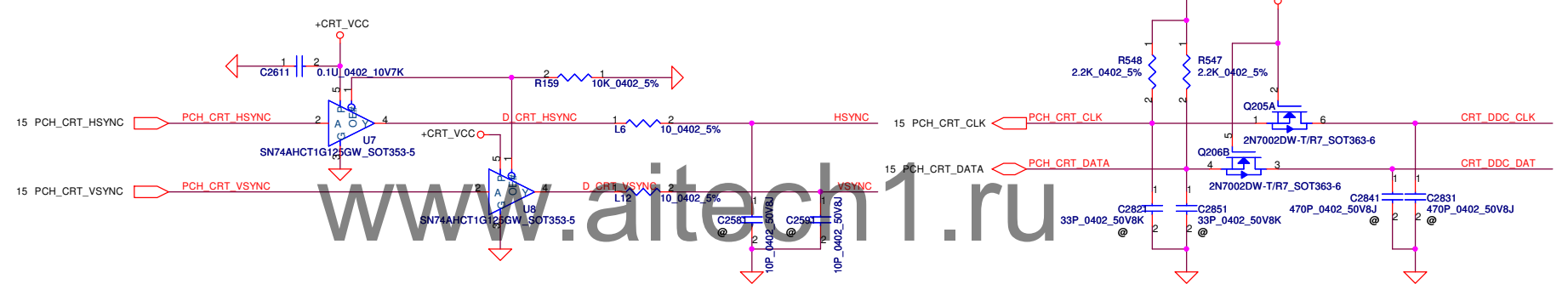
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		Size	Document Number	LA-8711	
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CRT CONNECTOR



USE old footprint need update
C-H_13-12201503CP_15P-T



For CRT

For HDMI

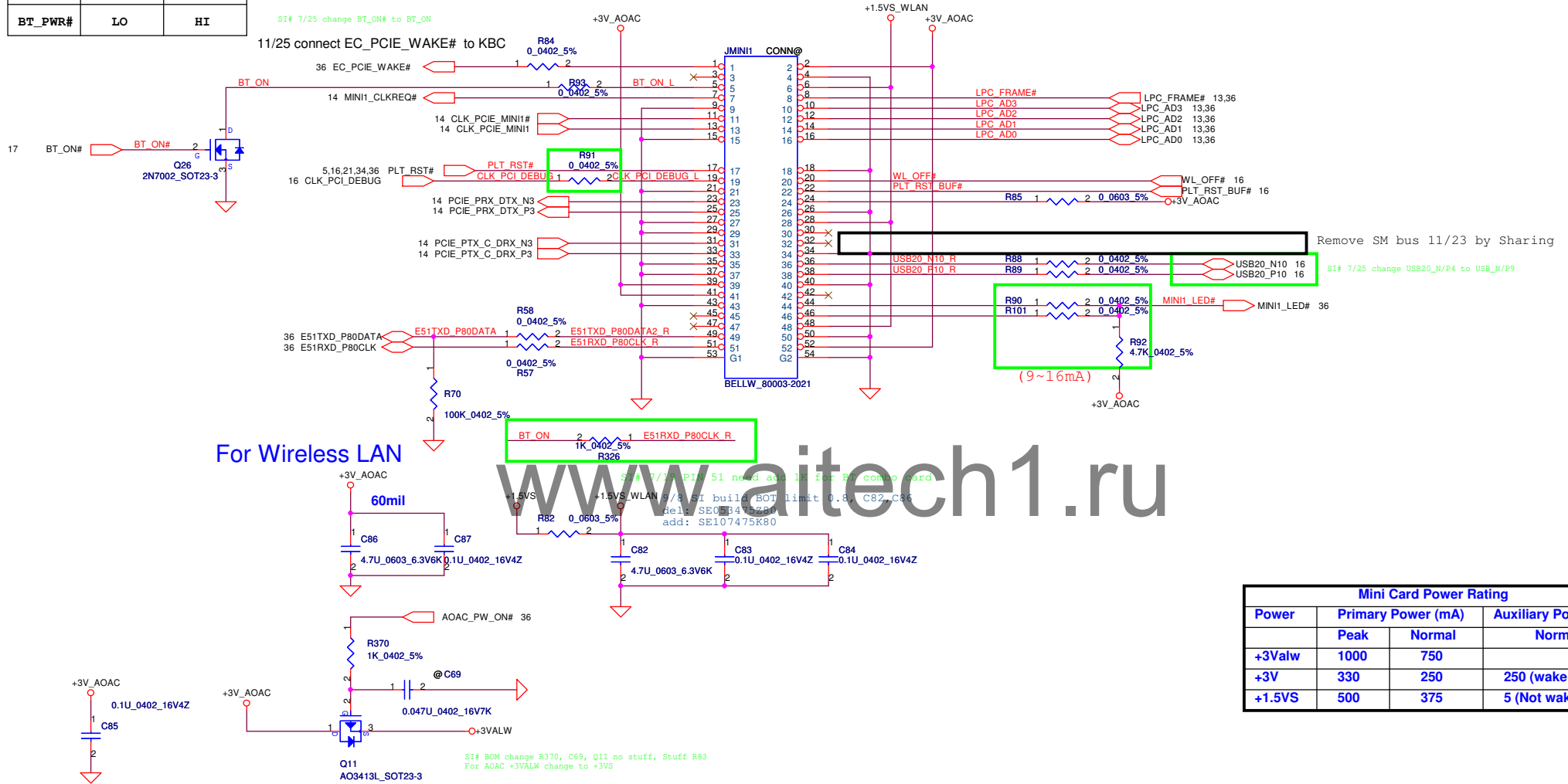
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Size		Document Number		Rev	
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LA-8711		0.1			

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

SI# 7/25 change BT_ON# to BT_ON

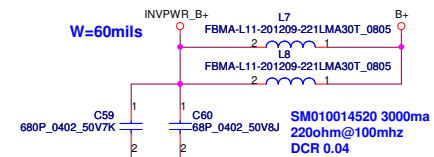
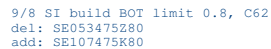
11/25 connect EC_PCIE_WAKE# to KBC



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3Valw	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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				Size Document Number
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				Date: Sunday, November 27, 2011
				Sheet 31 of 57

LCD POWER CIRCUIT



LCD/LED PANEL Conn.

W=60mils W=60mils

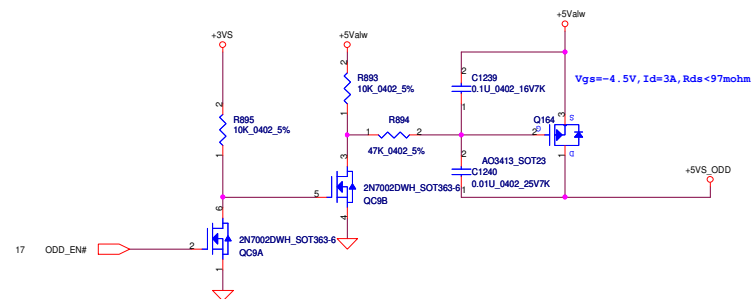
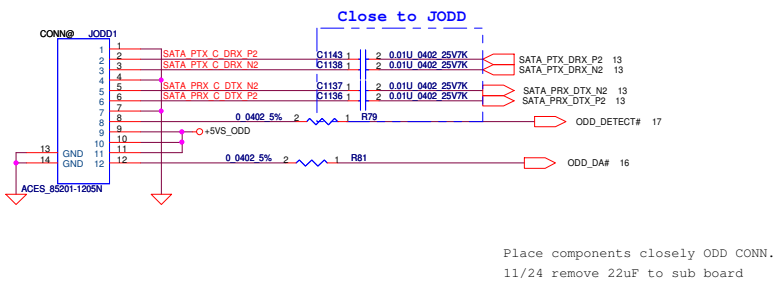
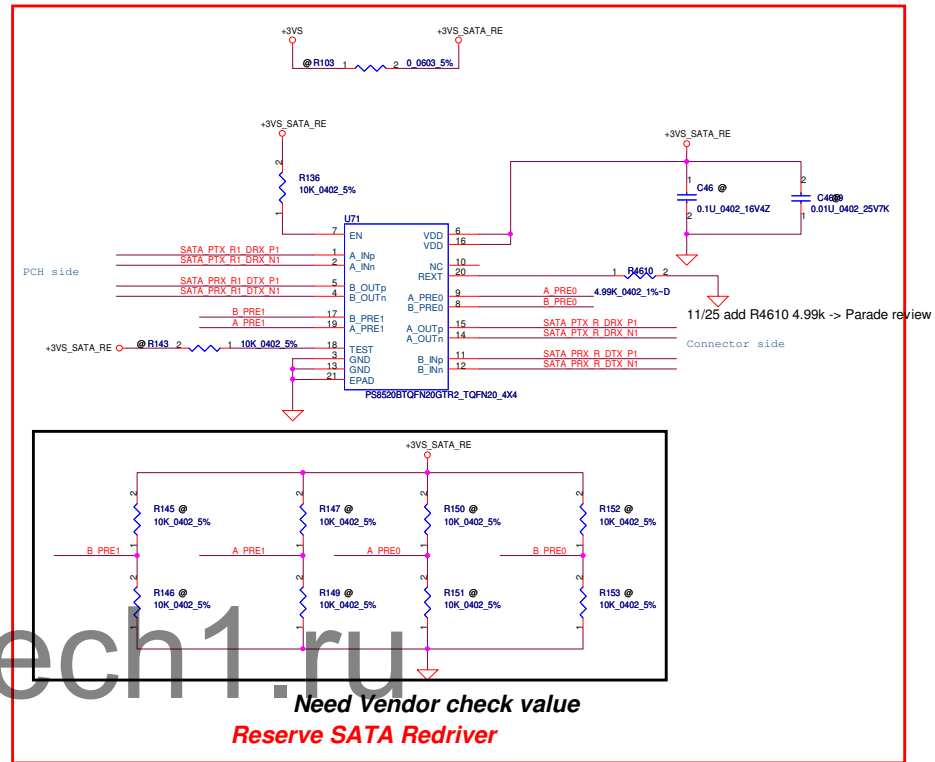
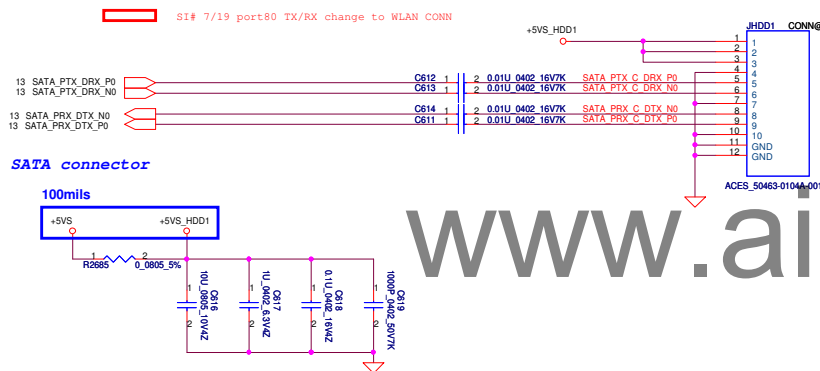
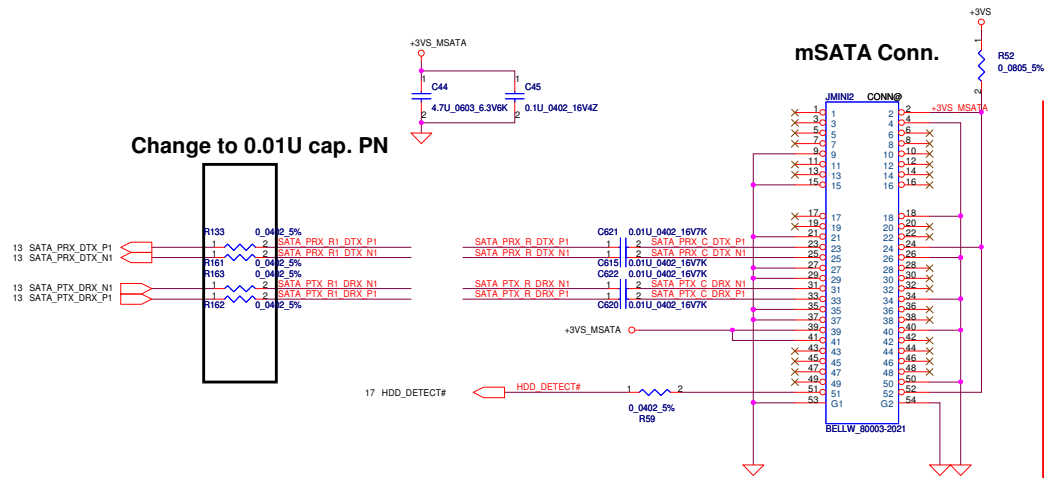


Pin connection diagram for the STARC_T11H30-000000-G4-R module. The diagram shows a 35-pin connector on the right, labeled JLVDS1, connected to various components on the left. Power pins include +LVDVDD (pin 1), +3VSD (pin 27), and GND (pins 31-35). Signal pins include LCD_CLK (pin 4), LCD_DATA (pins 5-7), PCH_TXOUT0+/- (pins 15, 16), PCH_TXOUT1+/- (pins 11, 12), PCH_TXOUT2+/- (pins 13, 14), PCH_TXCLK+/- (pins 17, 18), USB20_N8_R (pin 19), USB20_P8_R (pin 20), DISPOFF# (pin 21), INVPWM (pin 22), D_MIC_CLK (pin 28), and D_MIC_DATA (pins 29-30).

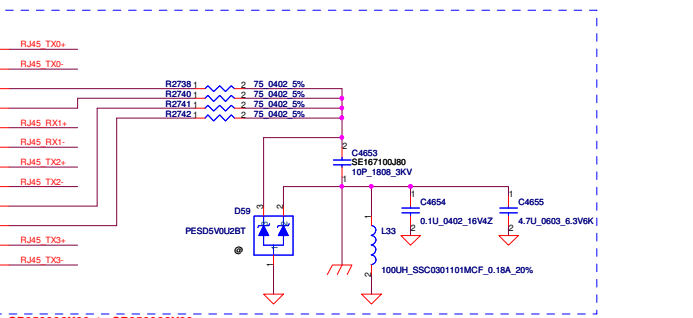
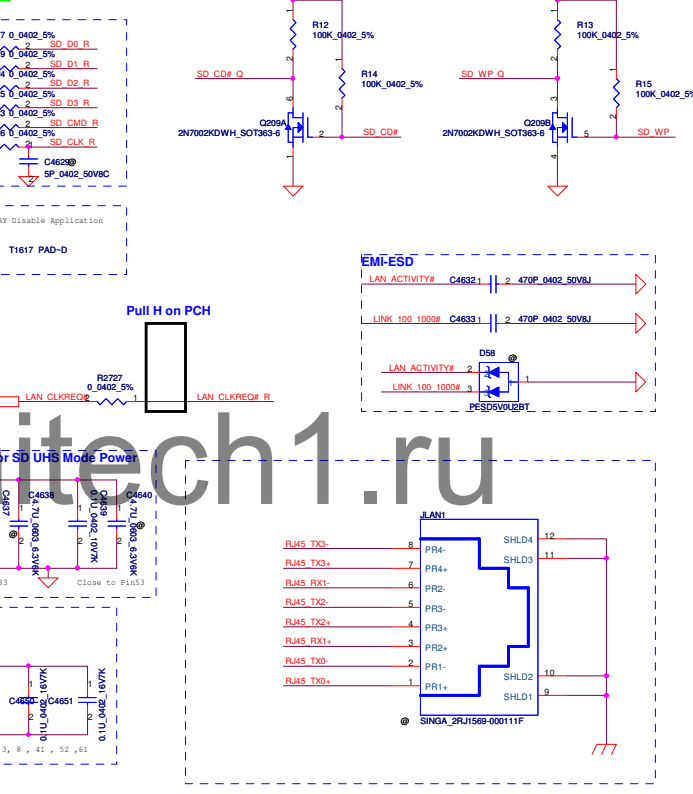
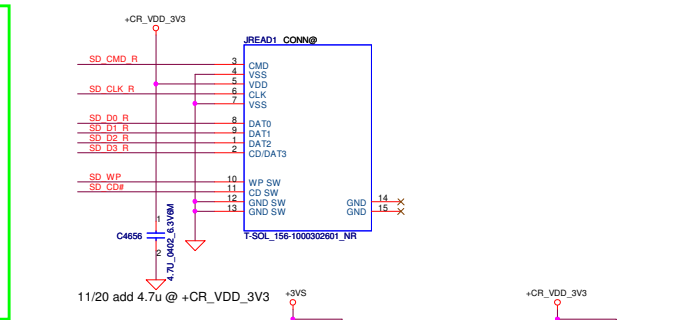
38 D_MIC_CLK_L_C D MIC CLK L C 100_040z_5% HA15 LA19 FBMA-P110-160808-301LMT_2P 2 D MIC CLK 1 D MIC CLK

38 D_MIC_DATA_C D MIC DATA C 2 D MIC DATA 2 D MIC DATA LA20 FBMA-L10-160808-301LMT_2P

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						LVDS Connector				
						Size	Document Number			
						Rev				
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Date:		Sunday, November 27, 2011		Sheet	32	of 57				

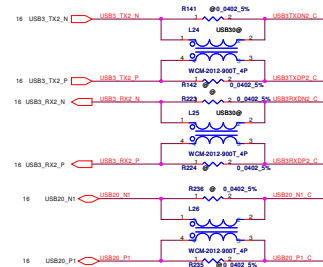
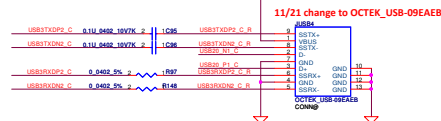
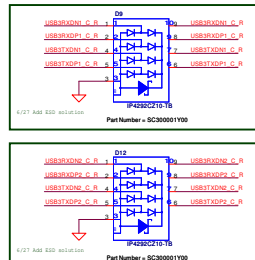
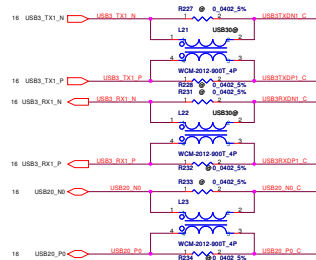
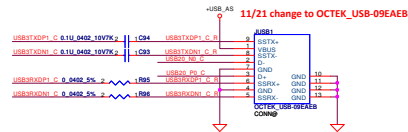
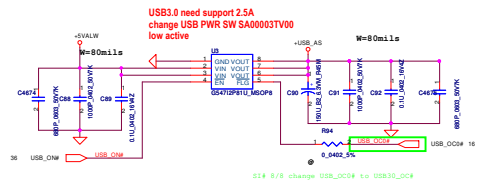


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					Size C	Document Number	Rev 0.1
					LA-8711		
Date:		Sunday, November 27, 2011		Sheet	33	of 57	



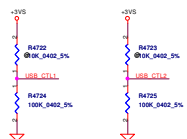
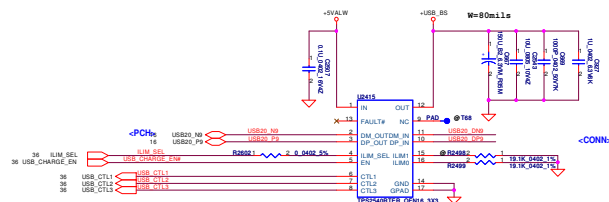
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USB3.0

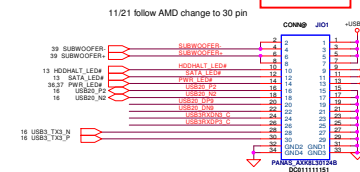
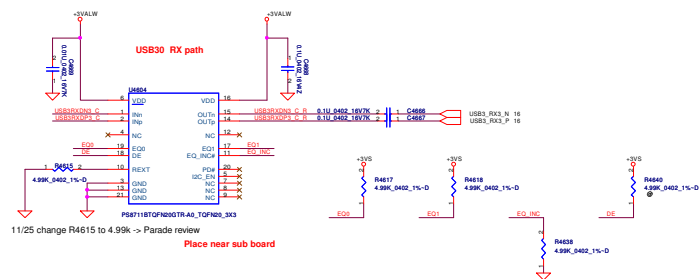


USB2.0 charger

USB charger footprint need change to TPS2543

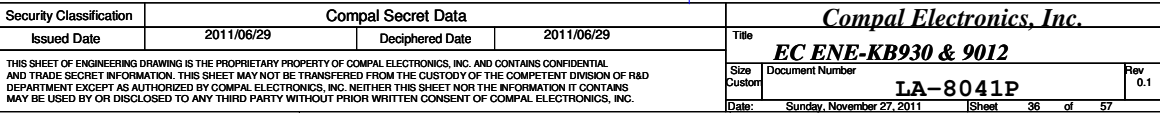


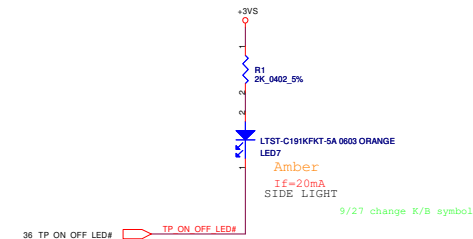
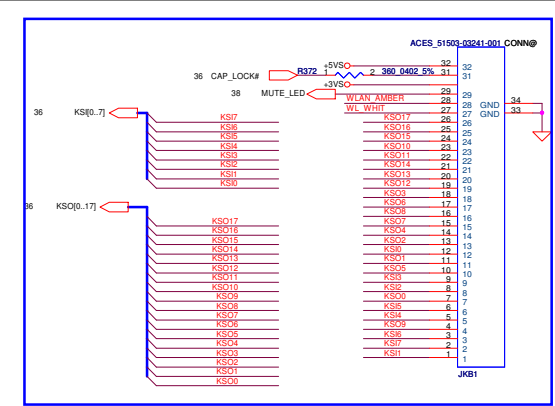
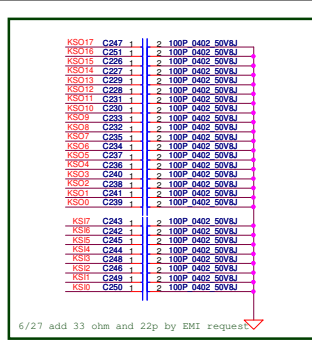
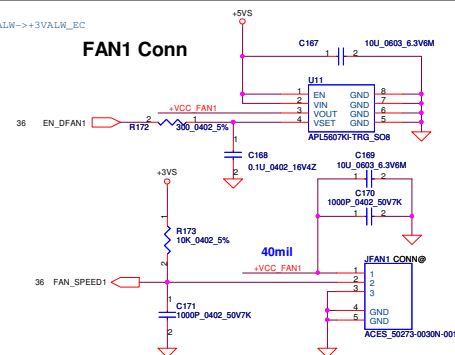
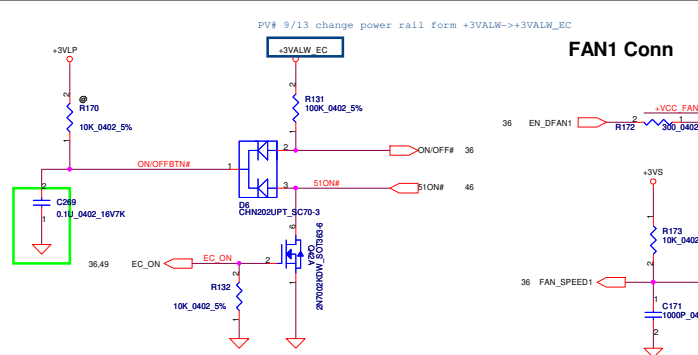
State	S0	S3, S4, S5
Mode	CDP	DCP
Control pin	CTL1 CTL2 CTL3 ILIM_SEL	CTL1 CTL2 CTL3 ILIM_SEL
	1 1 X 1	0 0 1 1



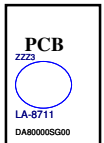
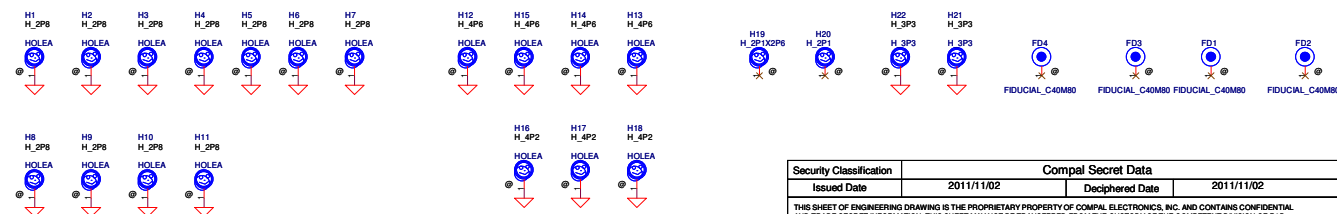
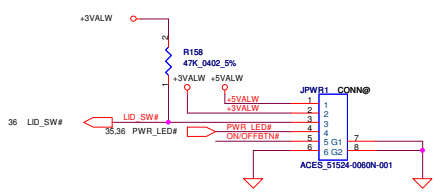
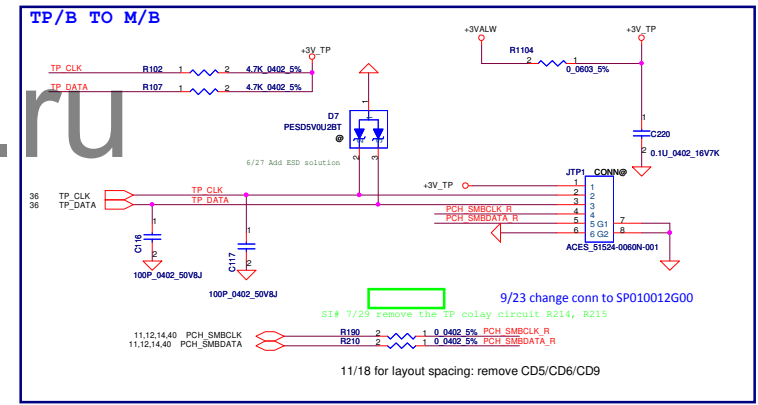
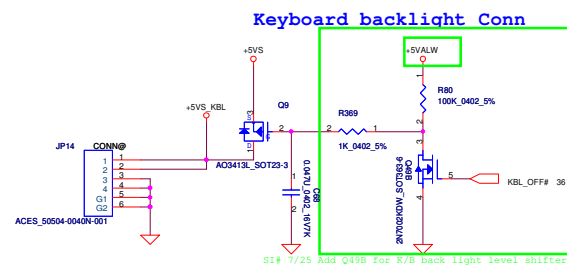
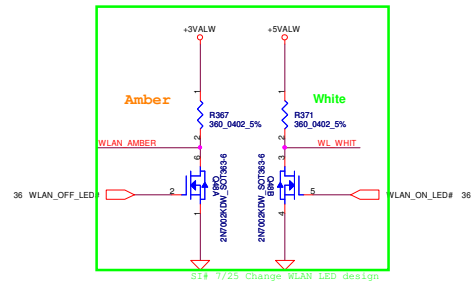
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Designed Date	2011/1/02	2011/1/02
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Rev	Rev	Rev
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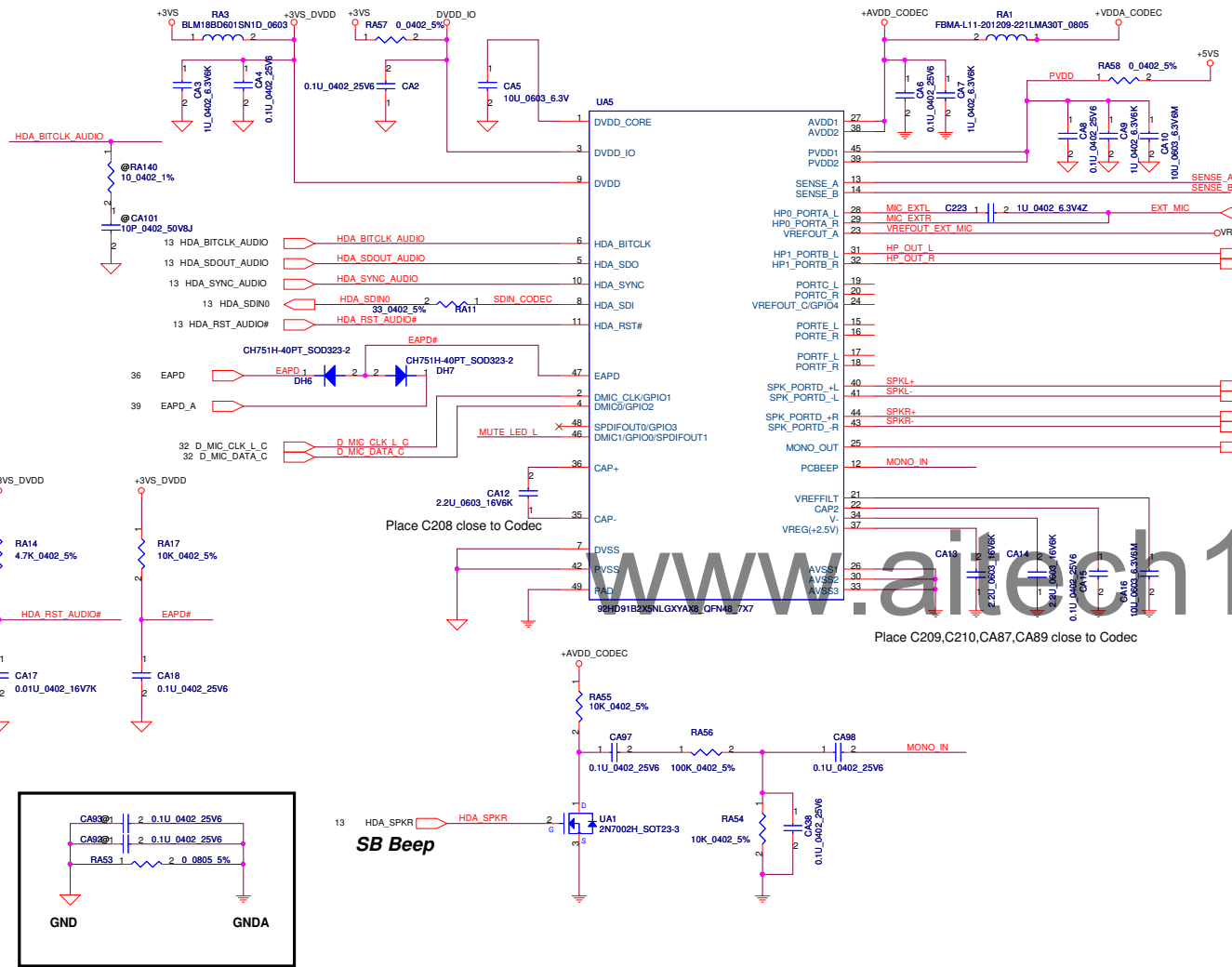
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				Date	Rev
				<p>LA-8041P</p>	0.1
				<p>Created: Sunday, November 27, 2011 1:08 PM</p>	4 of 57

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Place AVDD ,PVDD,and DVDD capacitor close to Codec

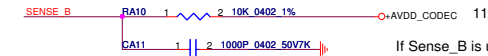
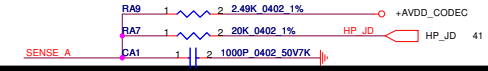
Notes:

Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than
6 inches, change C12 to 0.1uF

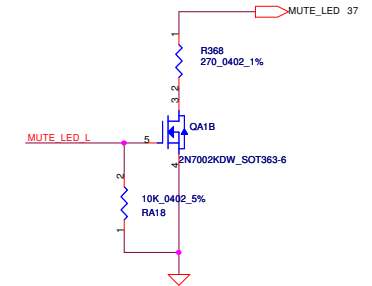


11/21 RA10 change to 10K(un-used)

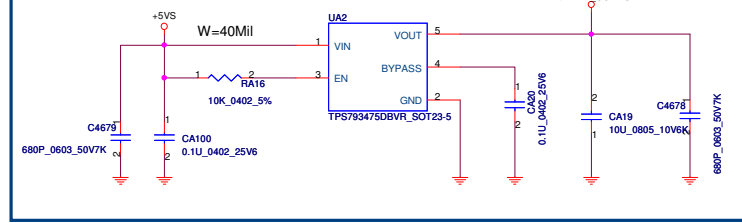
If Sense_B is un-used, then pull high
Sense_B to AVDD by 10Kohm resistor

HP Jack
Ext MIC

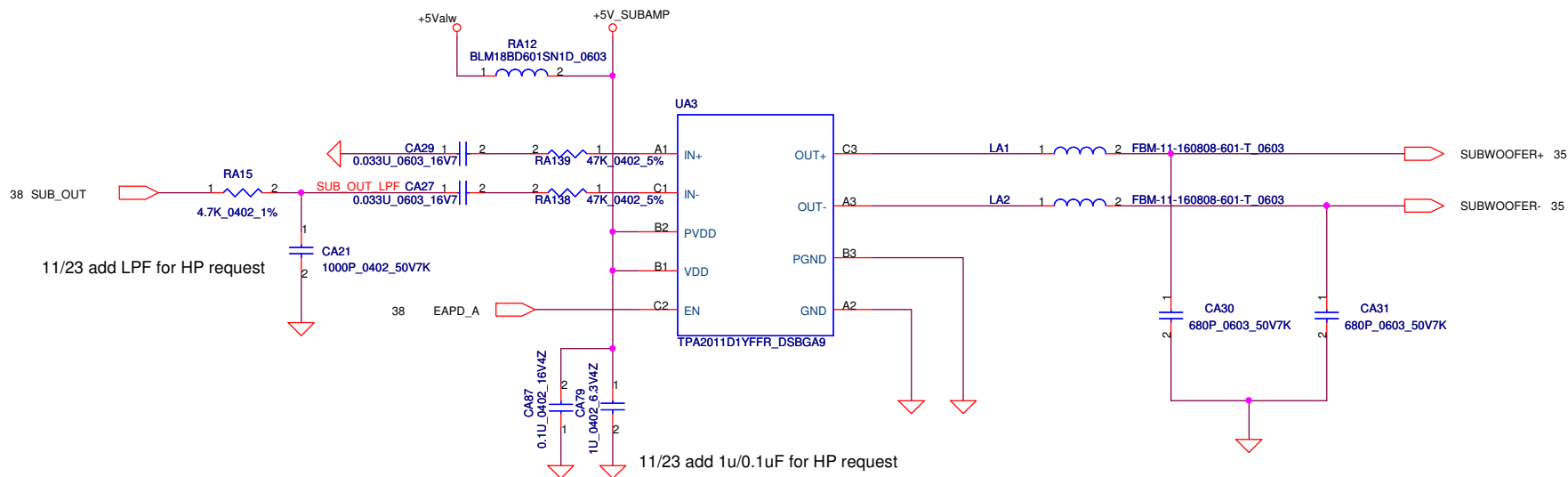
Internal SPKR
(front stereo speaker)



9/27 LDO TPS793475DBVR for audio power



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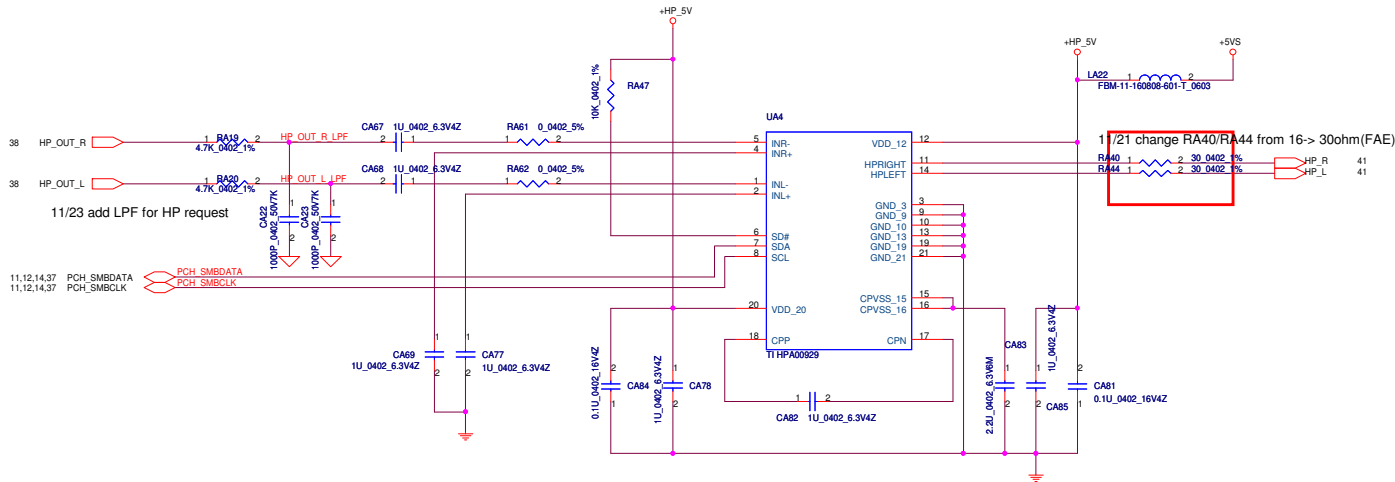


2011.10.28 Change Sub-woofer Amp to TPA2011D1

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				Size B	Rev 0.1
				Date:	Sunday, November 27, 2011
				Sheet	39 of 57

Headphone Amp

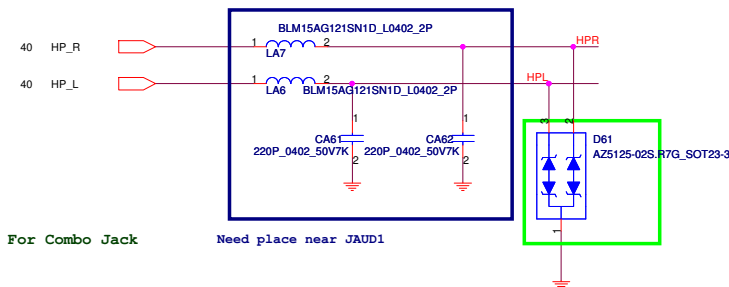
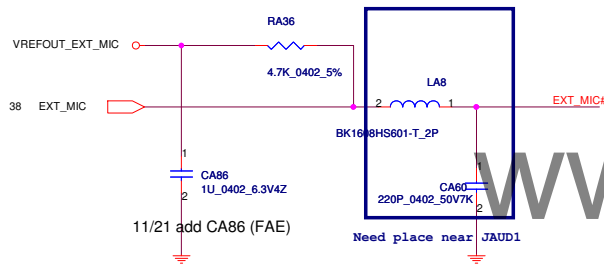
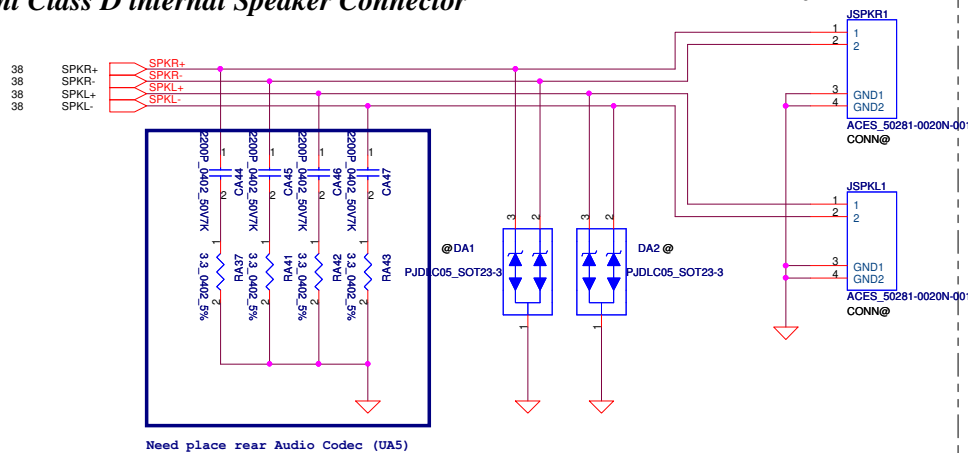


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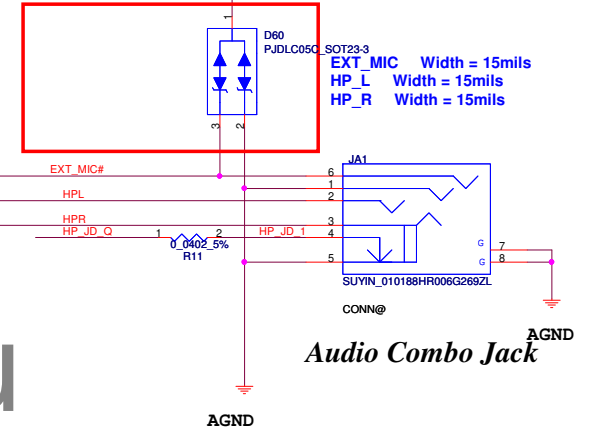
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				Size Document Number Custom
				Rev 0.1
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Front Class D internal Speaker Connector

11/25 change SPKR connector follw AMD

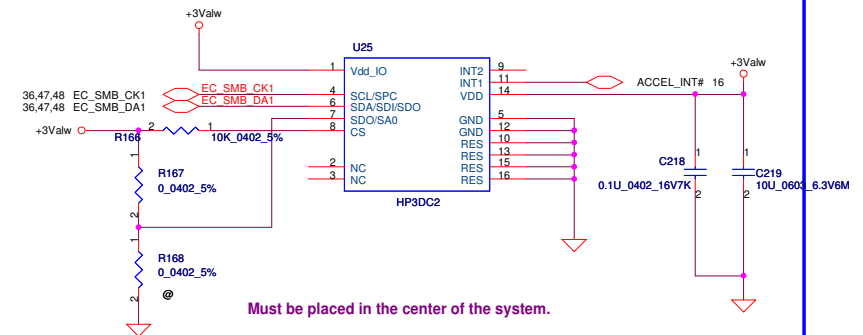


11/23 spacing concern: remove DA4/DA5, keep D60 only

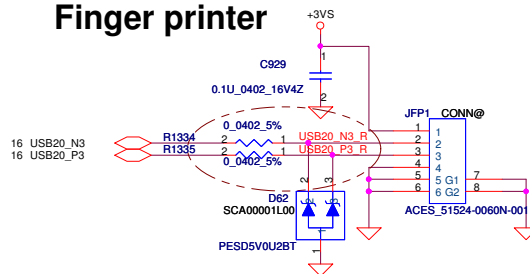


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ACCELEROMETER



Finger printer



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QC11 (LA-8551P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

	SOURCE	BATT	WLAN MINI1	mSATA MINI2	TP	SODIMM	EC_SMB_CLK2 PCH_SMB_CLK2	PCH_SMB_CLK PCH_SMB_DATA	G-Sensor	GPU	AMP
EC_SMB_CLK1 EC_SMB_DA1	KB930	V							V		
EC_SMB_CLK2 EC_SMB_DA2	KB930							V		V	
PCH_SMB_CLK PCH_SMB_DATA	PCH		@		V	V					V
PCH_SML_CLK PCH_SML_DATA	PCH						V			V	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	USB3.0 FL1009-2Q0		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI2
SATA1	m-SATA,JMINI1
SATA2	None
SATA3	None
SATA4	None
SATA5	None

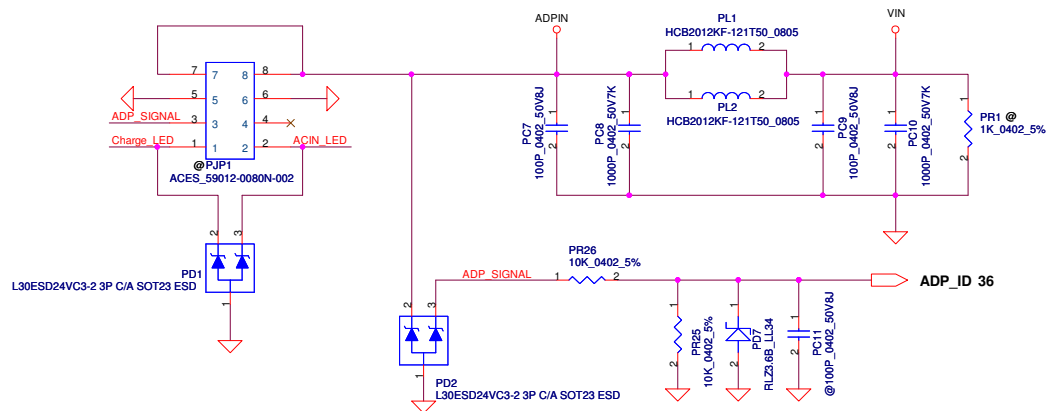
Option	@	CONN@	USB3.0@
UMA	X	X	V

USB Port Table

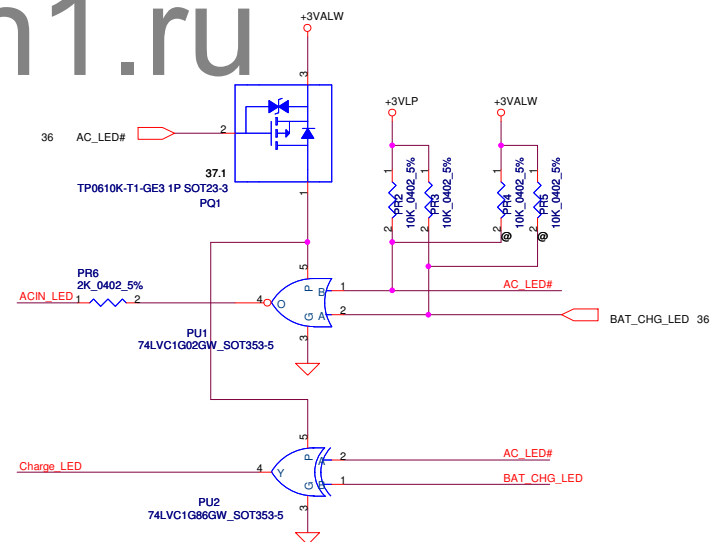
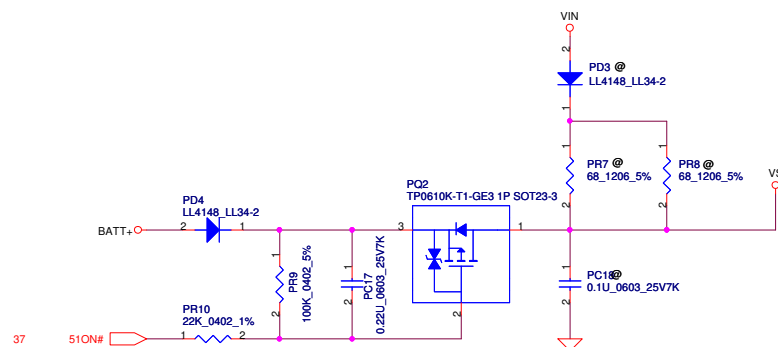
USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
		2	
	UHCI1	3	
		4	
	UHCI2	5	m-SATA
EHCI2		6	
	UHCI3	7	
		8	Camera
	UHCI4	9	Mini Card(WLAN)
		10	
	UHCI5	11	
		12	
	UHCI6	13	

USB 3.0	Port	1 External USB Port
	0	
	1	

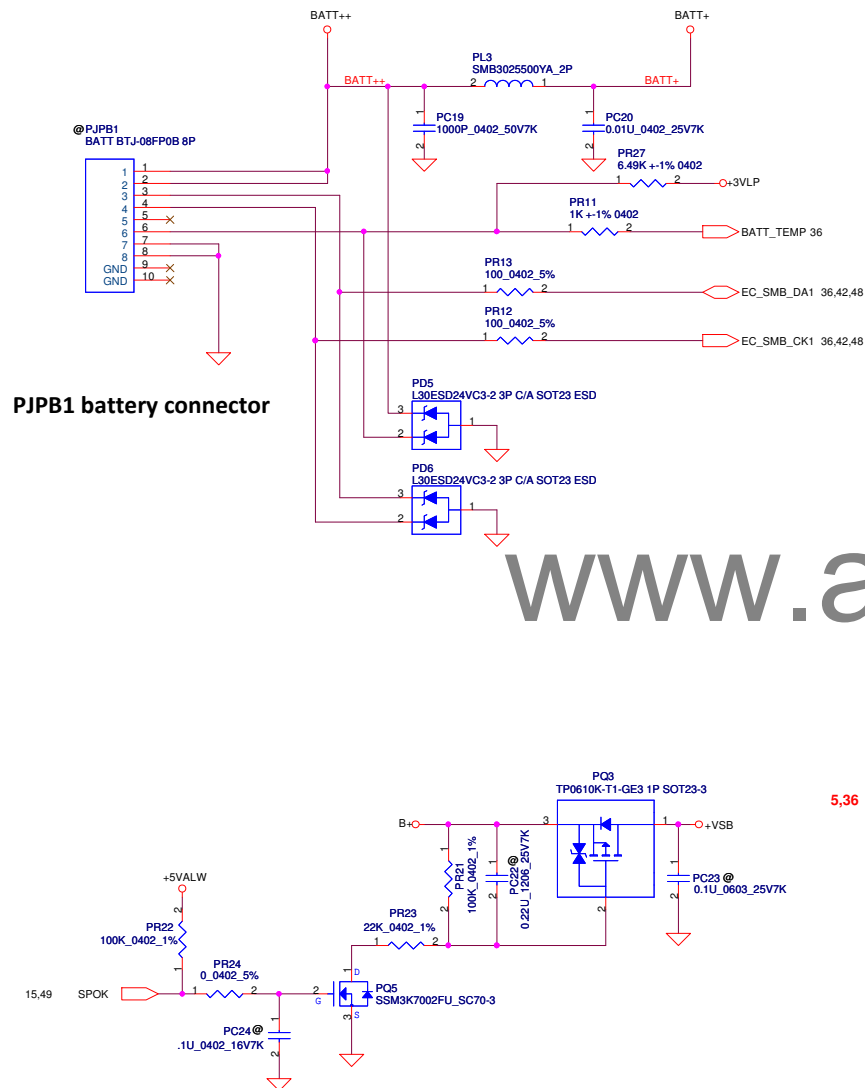
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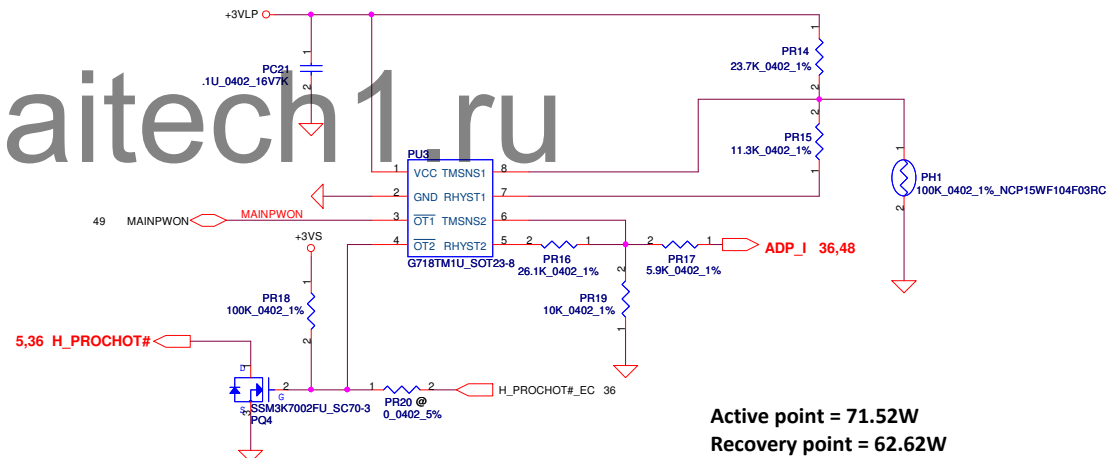


For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 --> Remove PU1 circuit, but keep PR25
PH1, PR15, PQ3, PR17, PR18, PR16
VCIN0_PH-->NTC_V
VCIN1_PH-->Turbo_V

PH1 under CPU bottom side :
CPU thermal protection at 90 +3 degree C
Recovery at 56 +3 degree C

$R_{set} = 3 * R_{tmh}$
 $R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$
 $R_{tmh} \text{ at } 90C = 7.8K, R_{tml} \text{ at } 56C = 26.1K$
 $R_{set} = 3 * 7.8K = 23.4K \Rightarrow 23.7K$
 $R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \Rightarrow 11.3K$



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2011/03/18
delete VIN voltage
detecting circuit

For KB930 --> Keep PR116

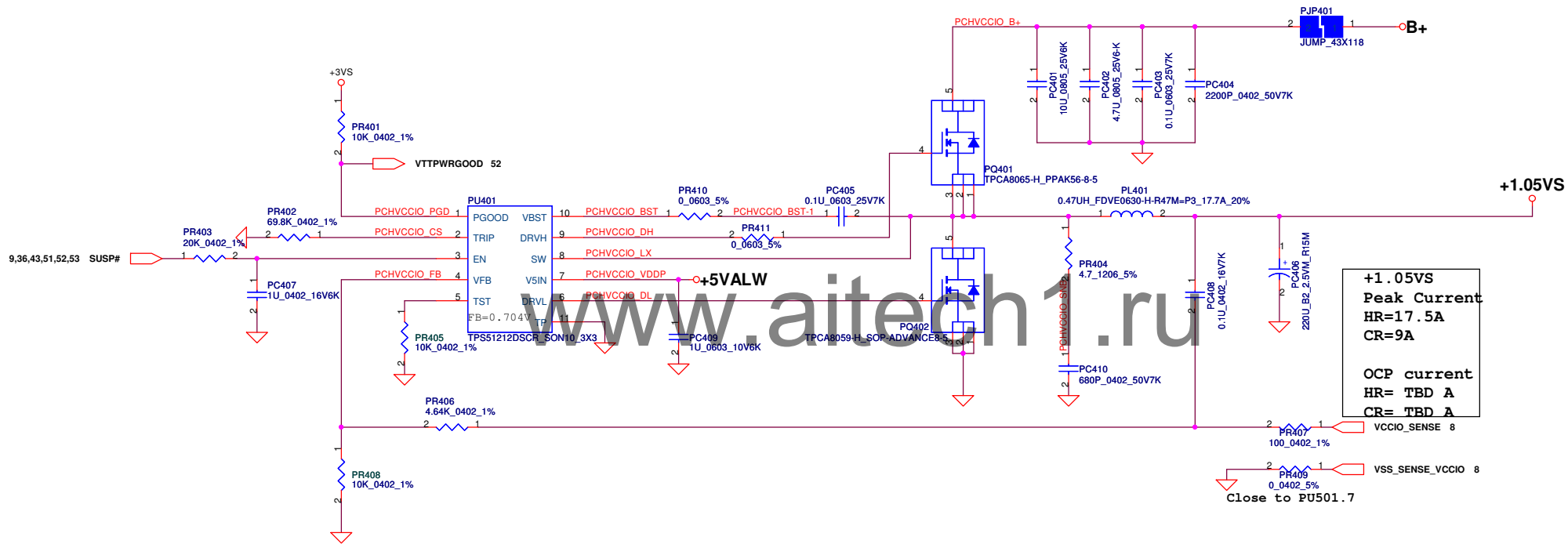
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For KB930 --> Keep PR116

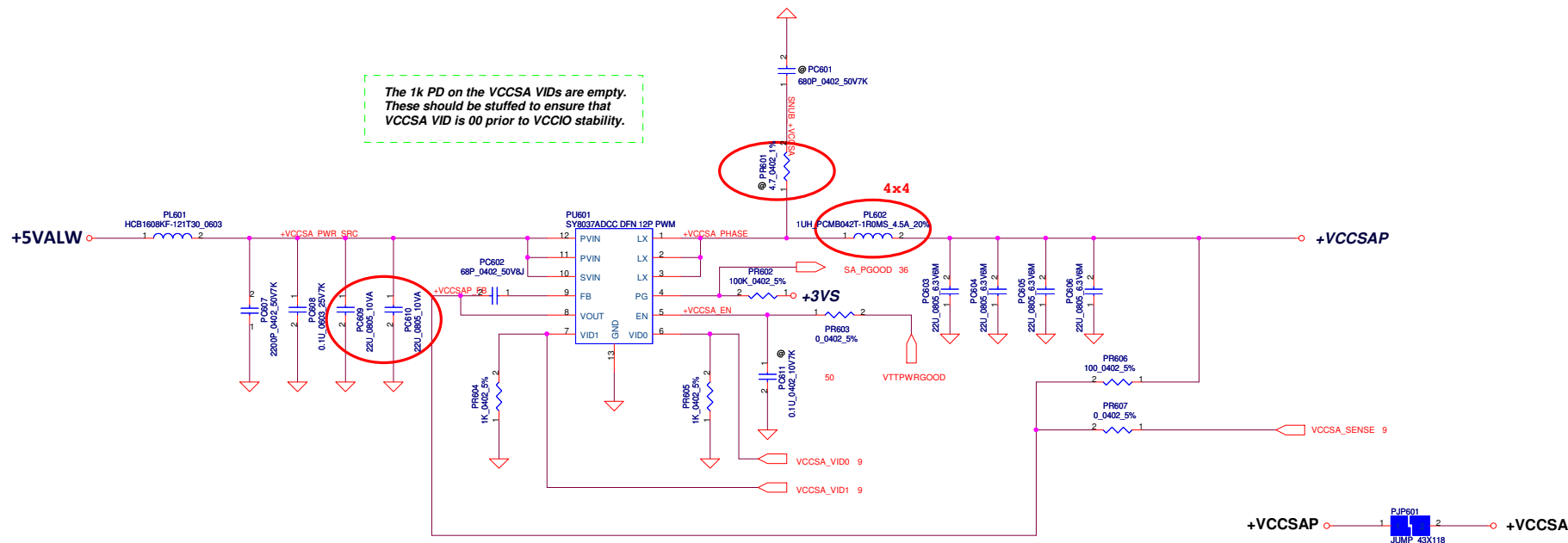
Min.	Typ	Max.
	17.33V	
	16.98V	

ILIM and external DPM
4.36A

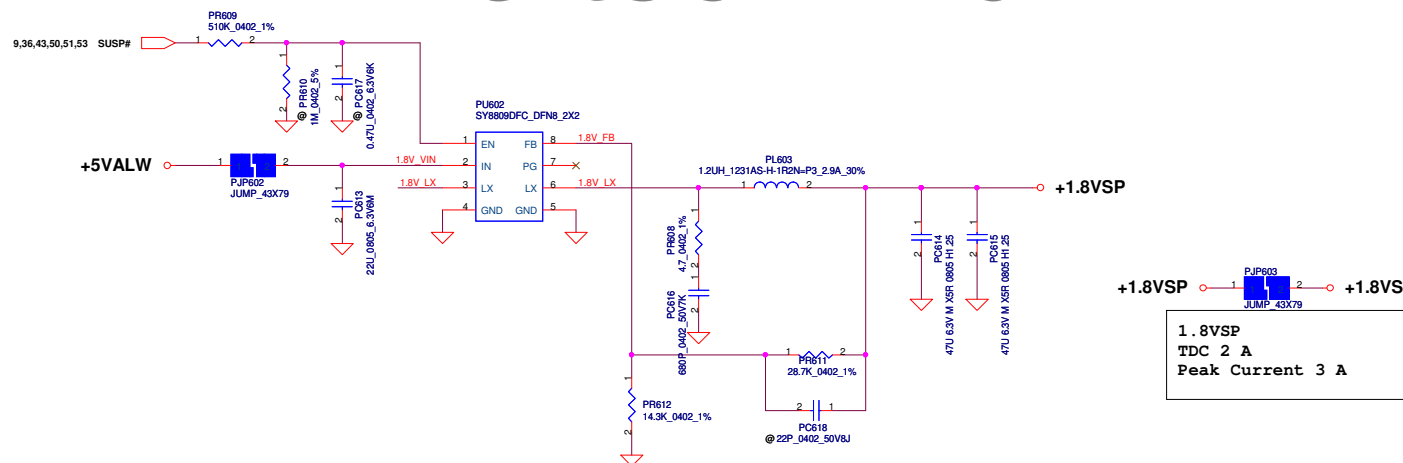
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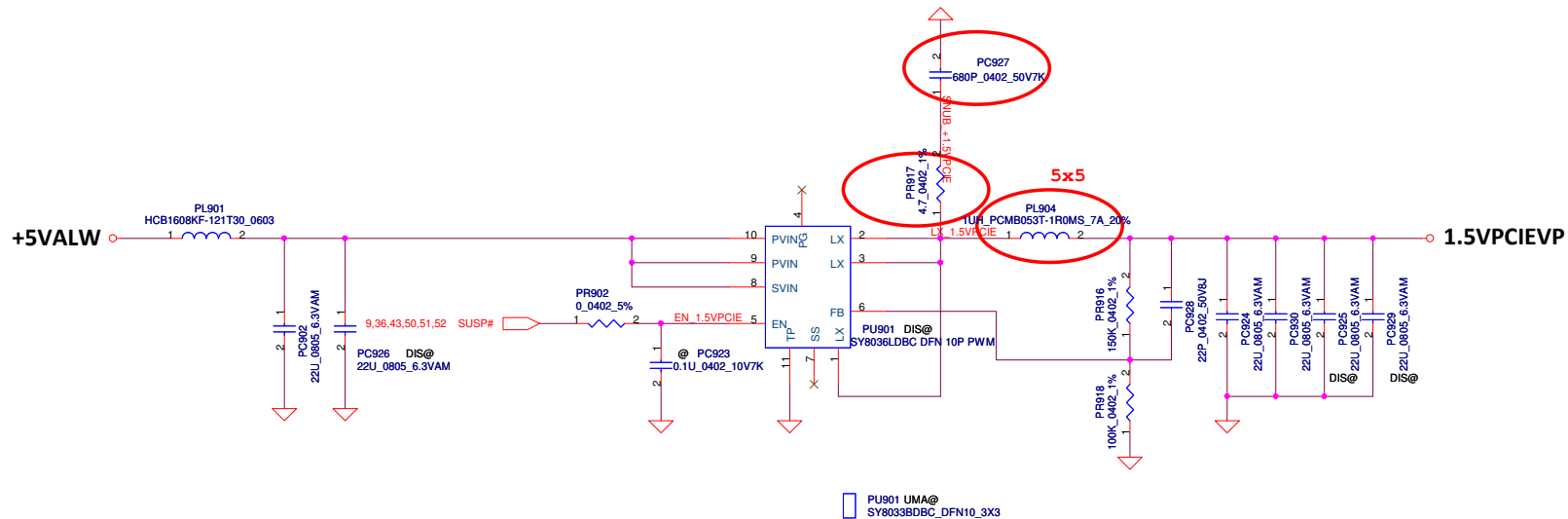
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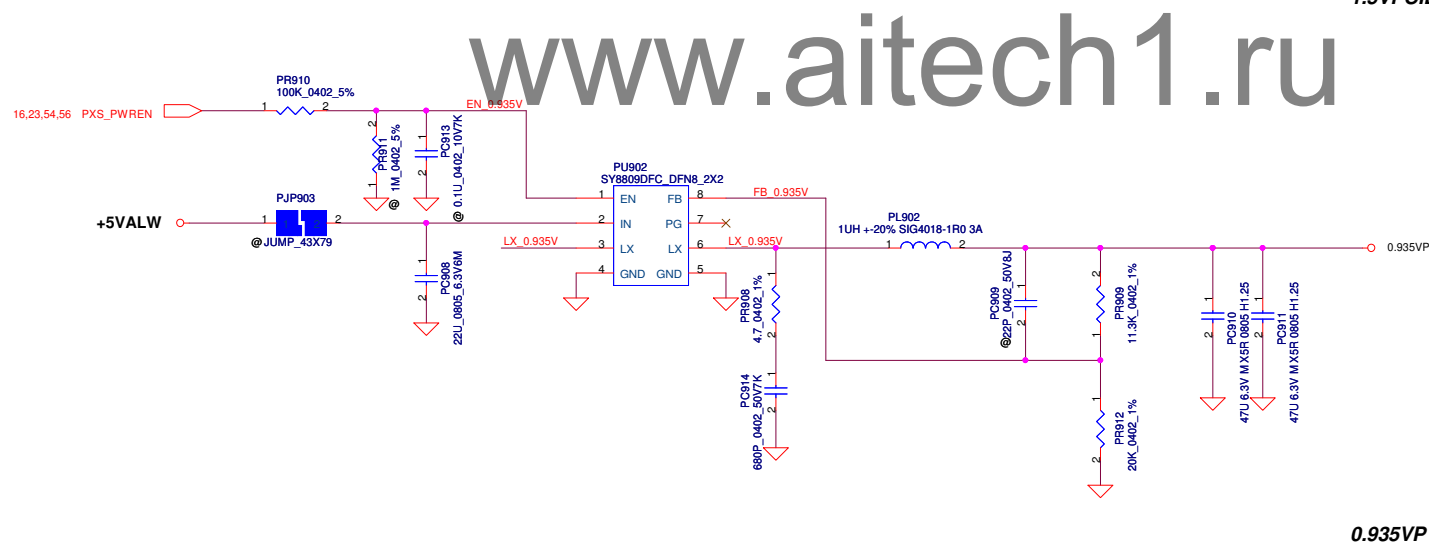


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1.5VPCIEVP

PJP902
@PAD-OPEN 4x4mm



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2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
 2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

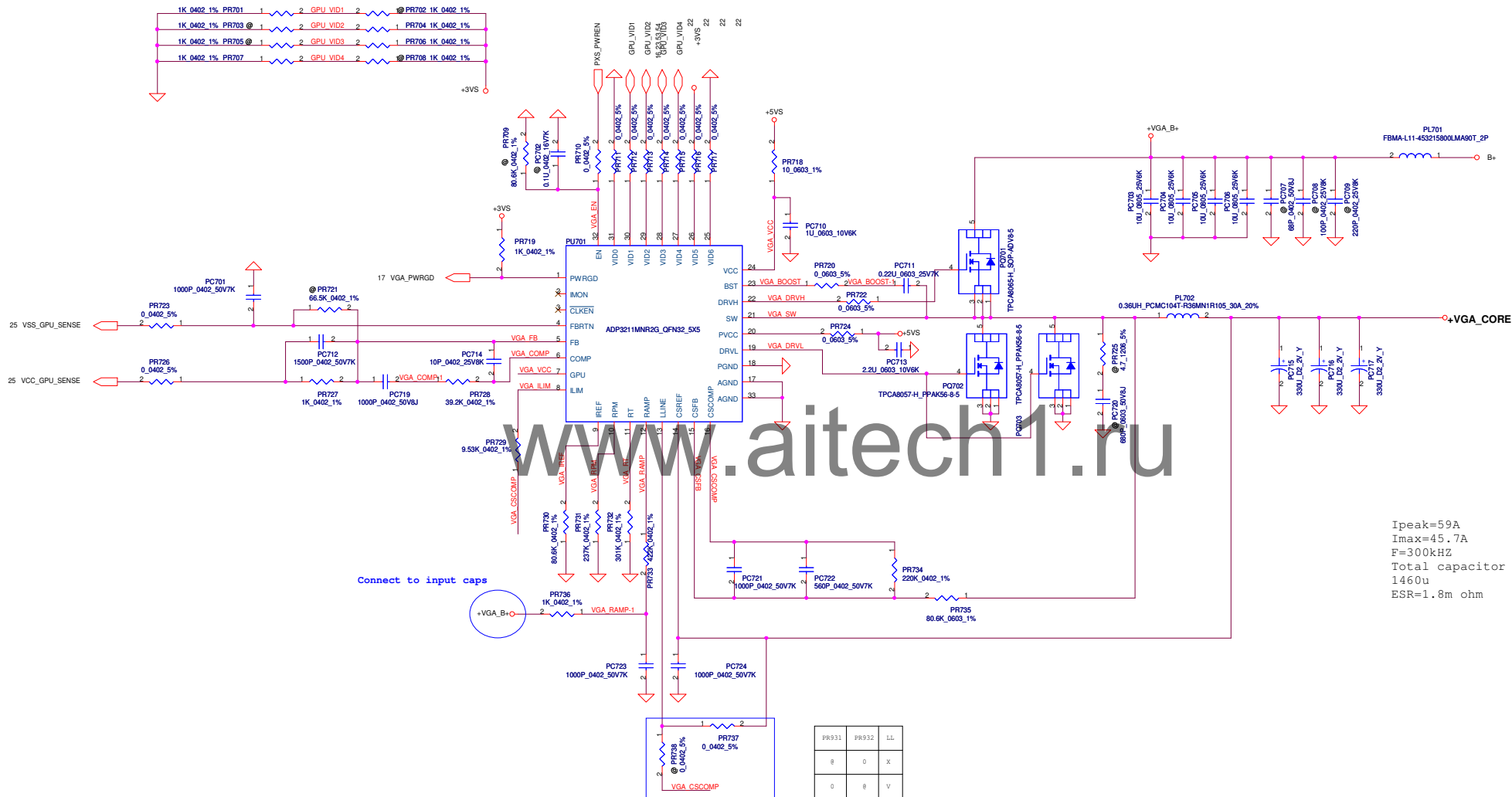
2-ph: PR178=1.47K for -70A OCP

+CPU_CORE
 Iccp=72A, IccMAX=53A
 Load line=1.9mohm
 DCR=1.1mohm

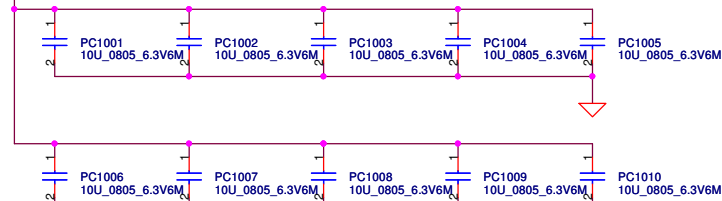
+GFX_CORE
 Iccp=40A, IccMAX=24A
 Load line=3.9mohm
 DCR=1.1mohm

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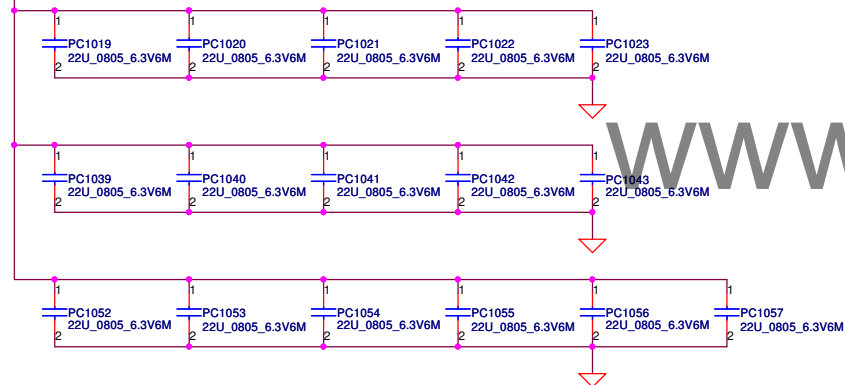
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Issued Date		2010/01/25		Deciphered Date		2009/04/28		Title	
								CPU_CORE/VGFX_CORE	
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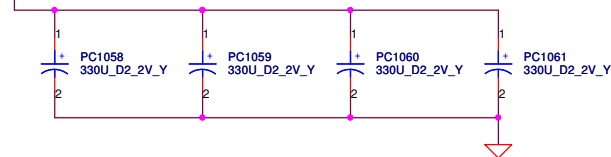
+CPU_CORE



+CPU_CORE



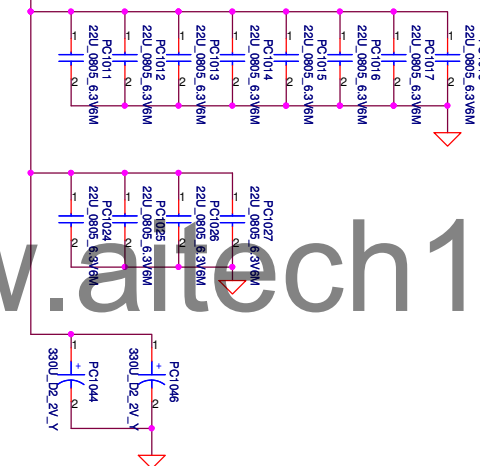
+CPU_CORE



+CPU_CORE

+VGFX_CORE

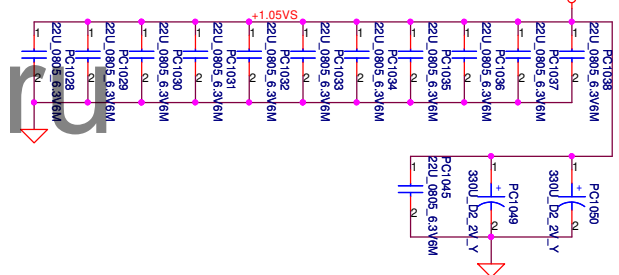
+VGFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05VS



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